High Performance Computing for fast tracking trigger at LHC/CMS

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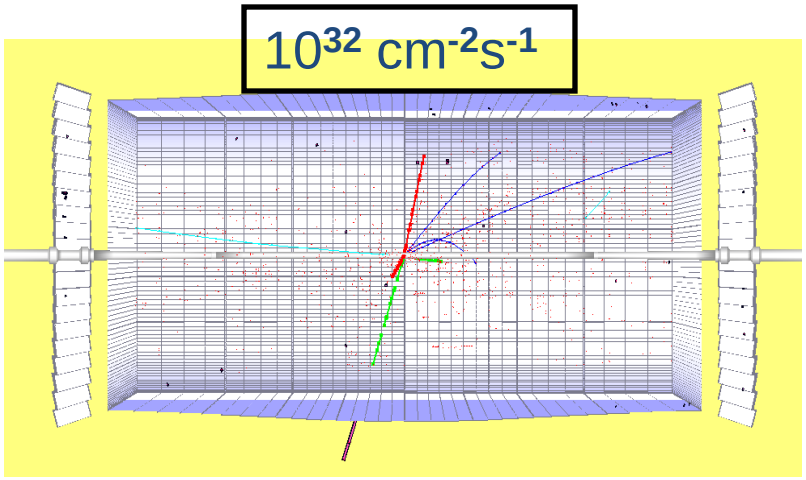
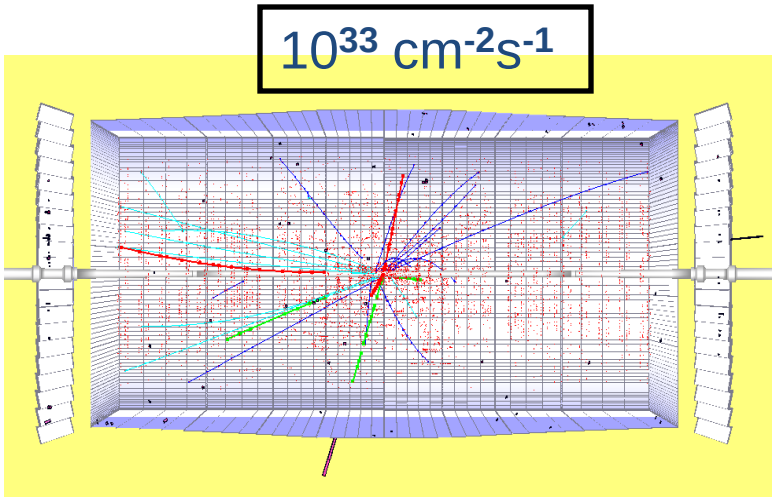
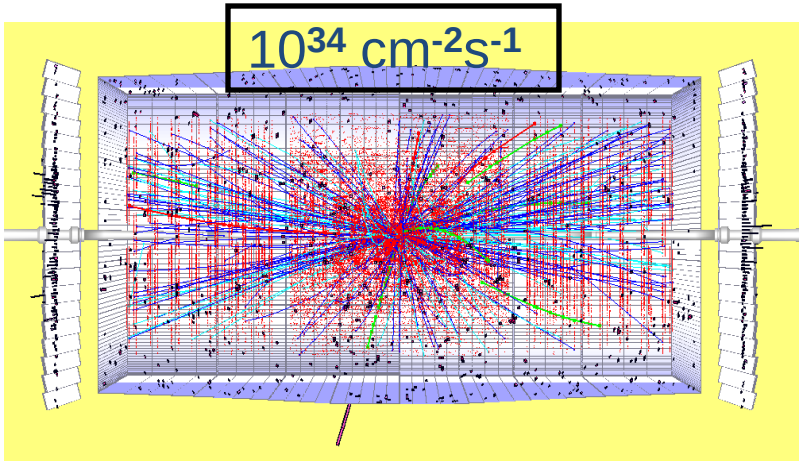
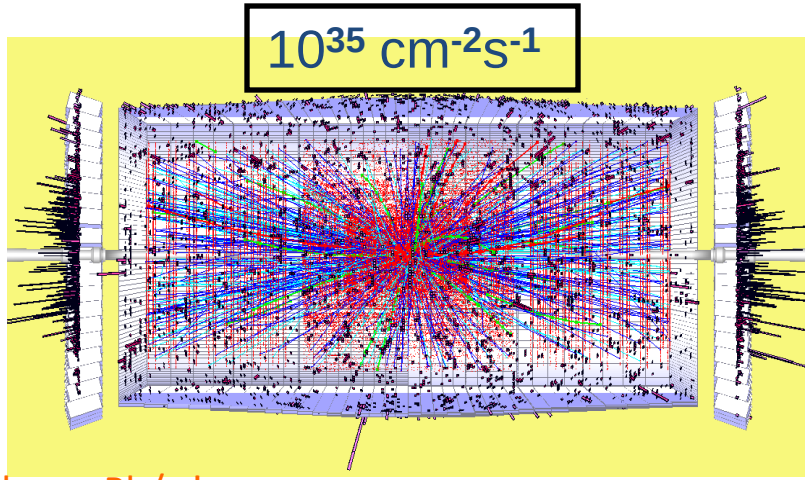
QuarkNet

Challenges at High Luminosity Large Hadron Collider (HL-LHC)







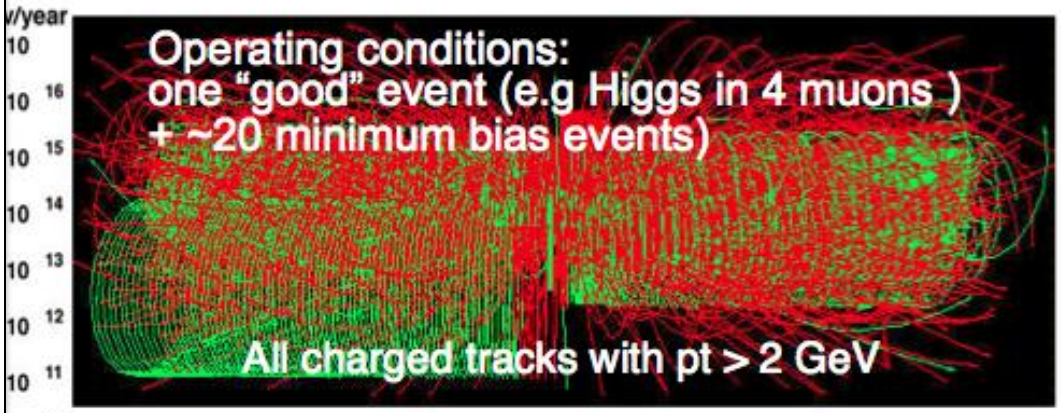


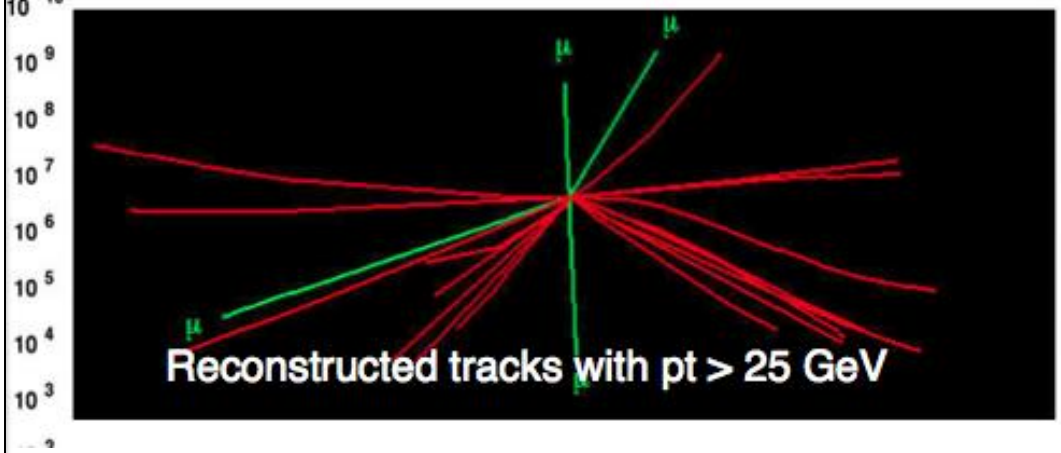
Raw information from silicon detector/tracker reaches ~ Pb/s !
at Phase II luminosity

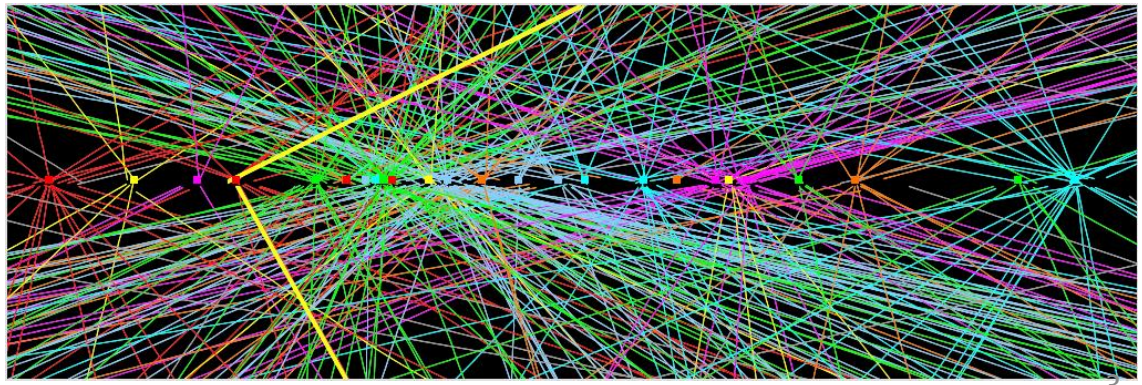
Will need to reconstruct charged particle trajectories "on-the-fly" for every beam crossing (25 ns, or 40 Million beam crossings per second), from an ocean of input data at up to ~ 100Tb/s.

This requires extremely fast high bandwidth data communication as well as massive pattern recognition power, with billion of known patterns to be compared against the multiple input data streams simultaneously with near zero latency.

and Fermilab has been developing this special system…







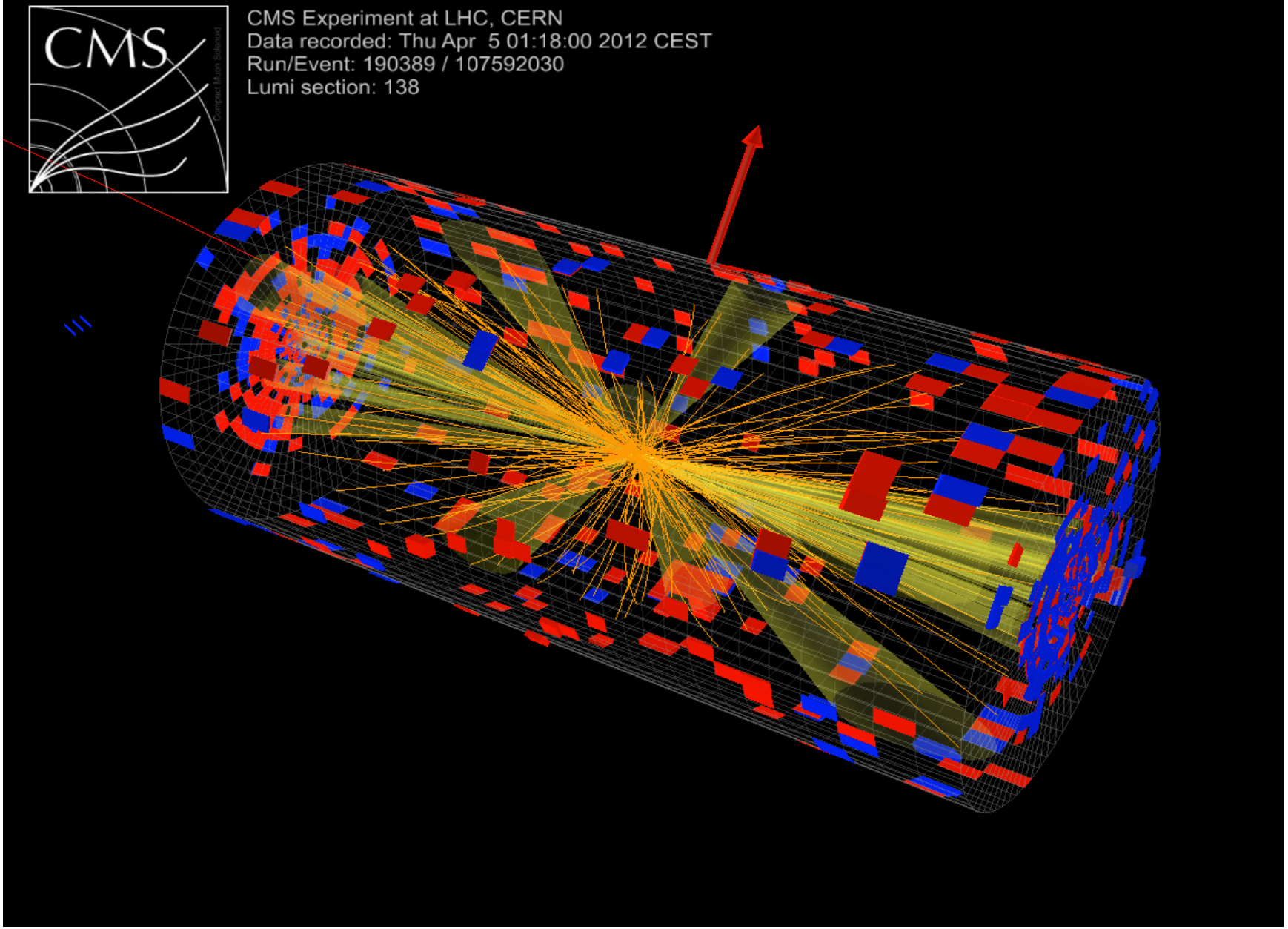
From "Trigger Challenges at High Luminosity LHC" by Ted Liu

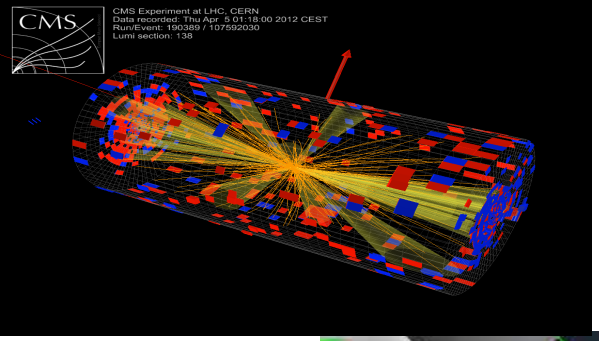
High Performance Computing

→ from "Report to the President and Congress" by President's Council of Advisors on Science and Technology, Dec. 2010 (page 65)

- Compute-intensive
  - massively parallel computation involving *very large number of processing elements*;
- Communication-intensive
  - *high-speed transfer of data* among processing elements;
- Data-intensive
  - *high-speed manipulation of* very large quantities of data

HL-LHC L1 Tracking Trigger is High Performance Computing
(Non-von Neumann approach)
Low Latency and Real Time


CMS
CMS Experiment at LHC, CERN
Data recorded: Thu Apr 5 01:18:00 2012 CEST
Run/Event: 190389 / 107592030
Lumi section: 138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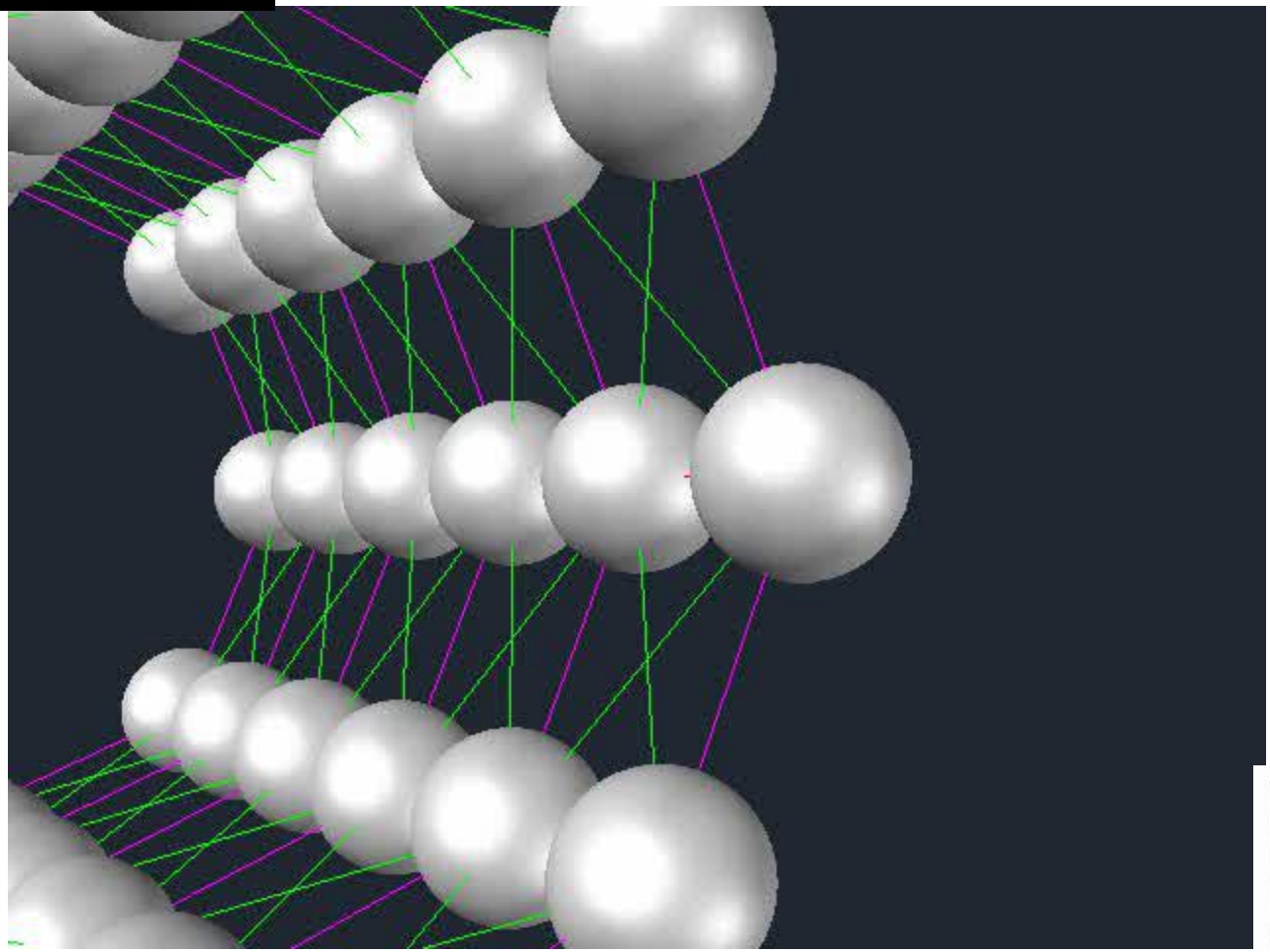
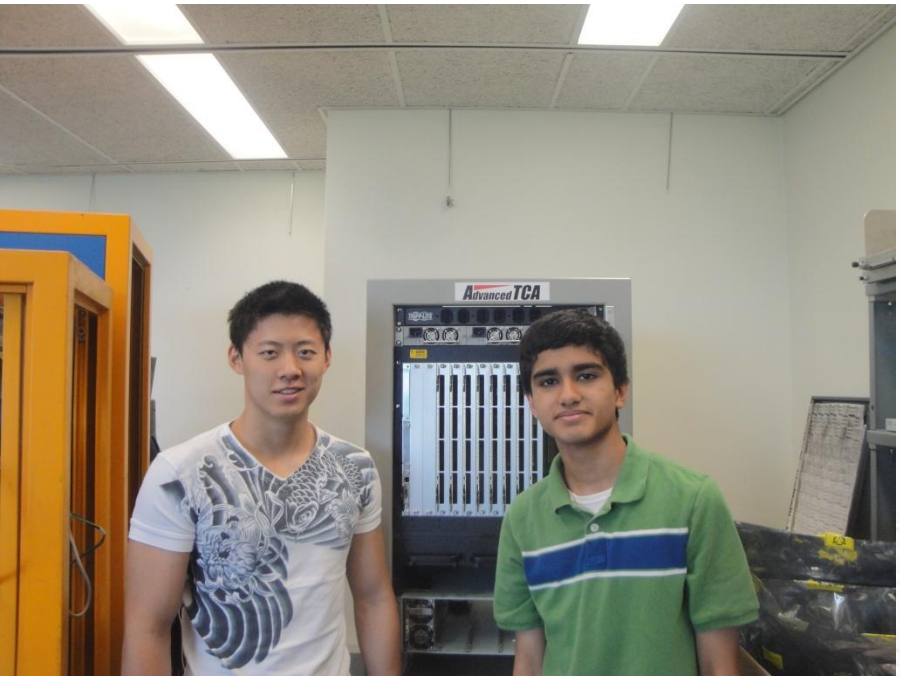
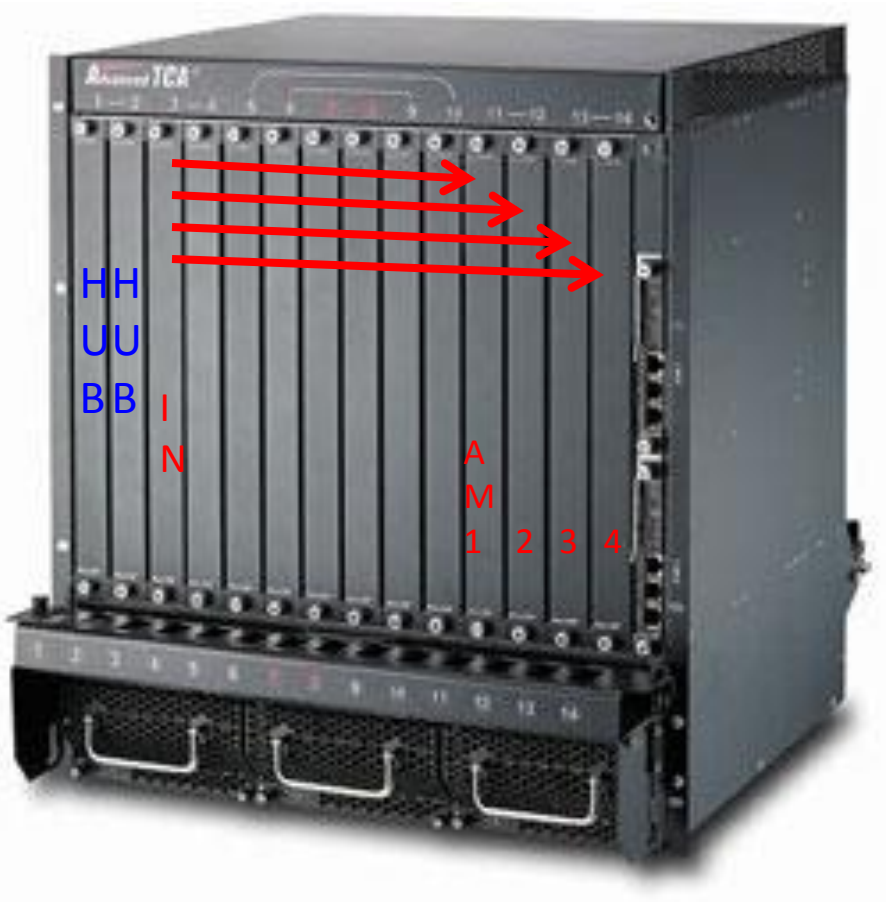


Crate/board level

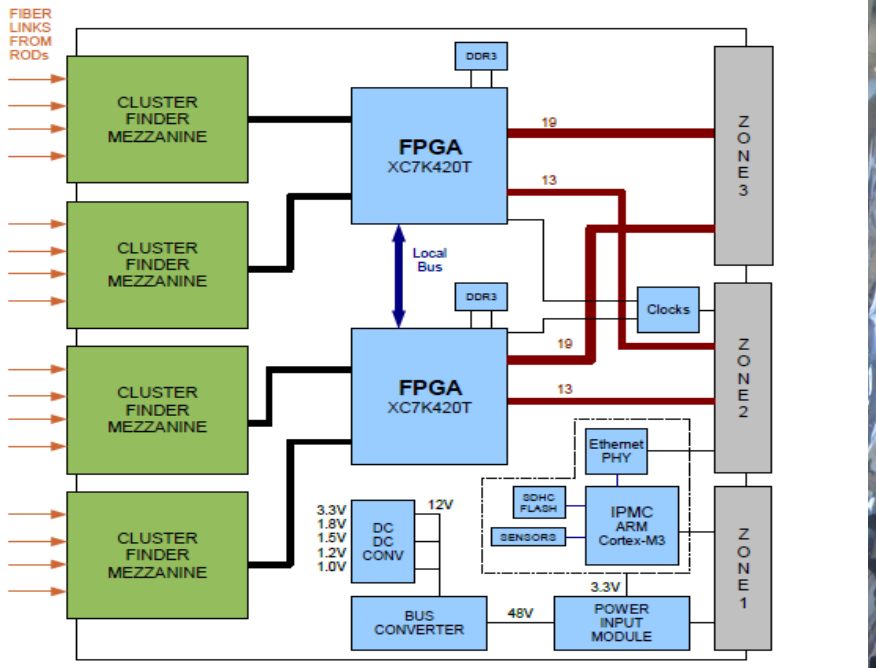
Dividing Detector region into smaller sectors in which each crate will correspond to one of the sectors.

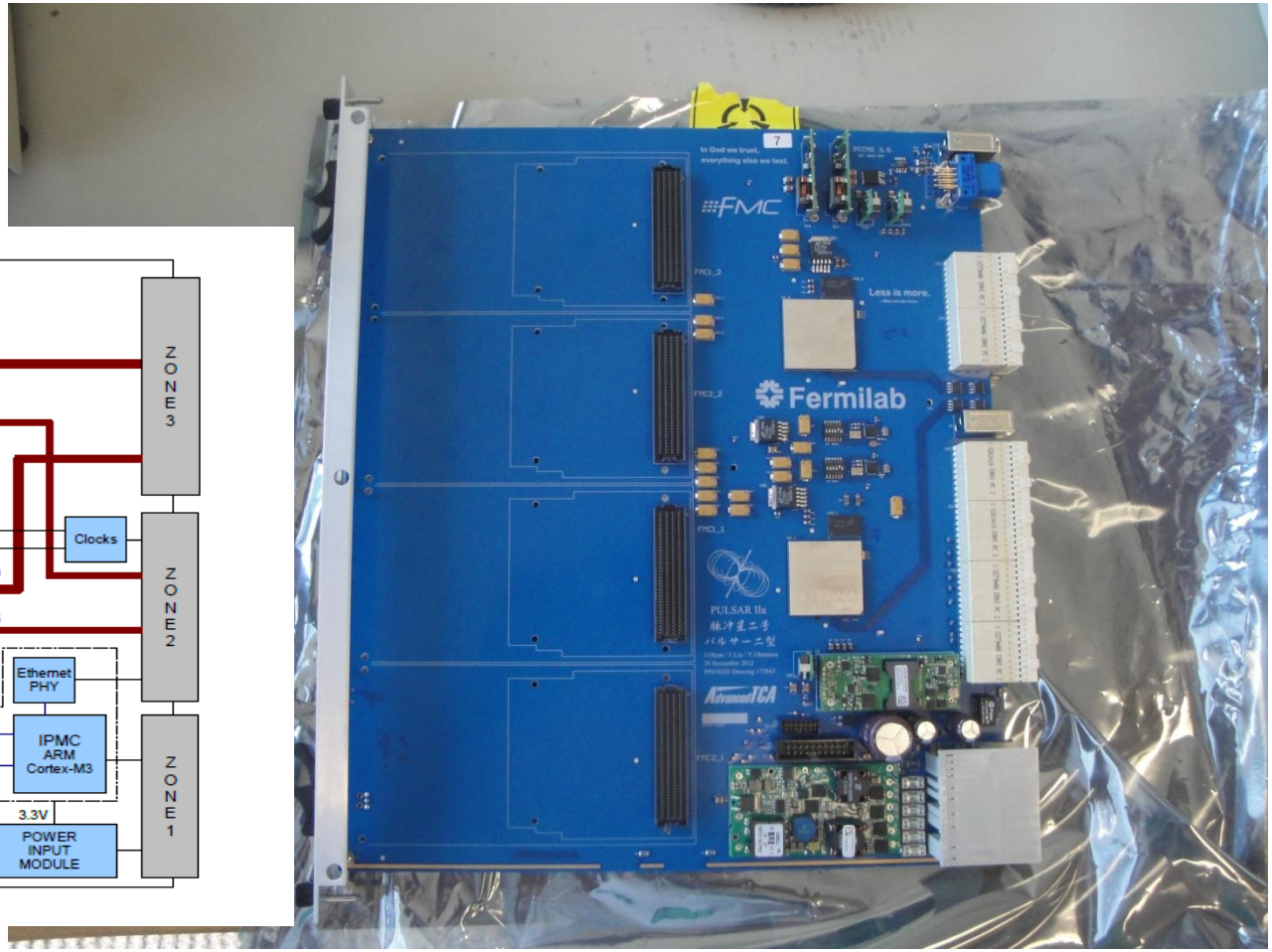


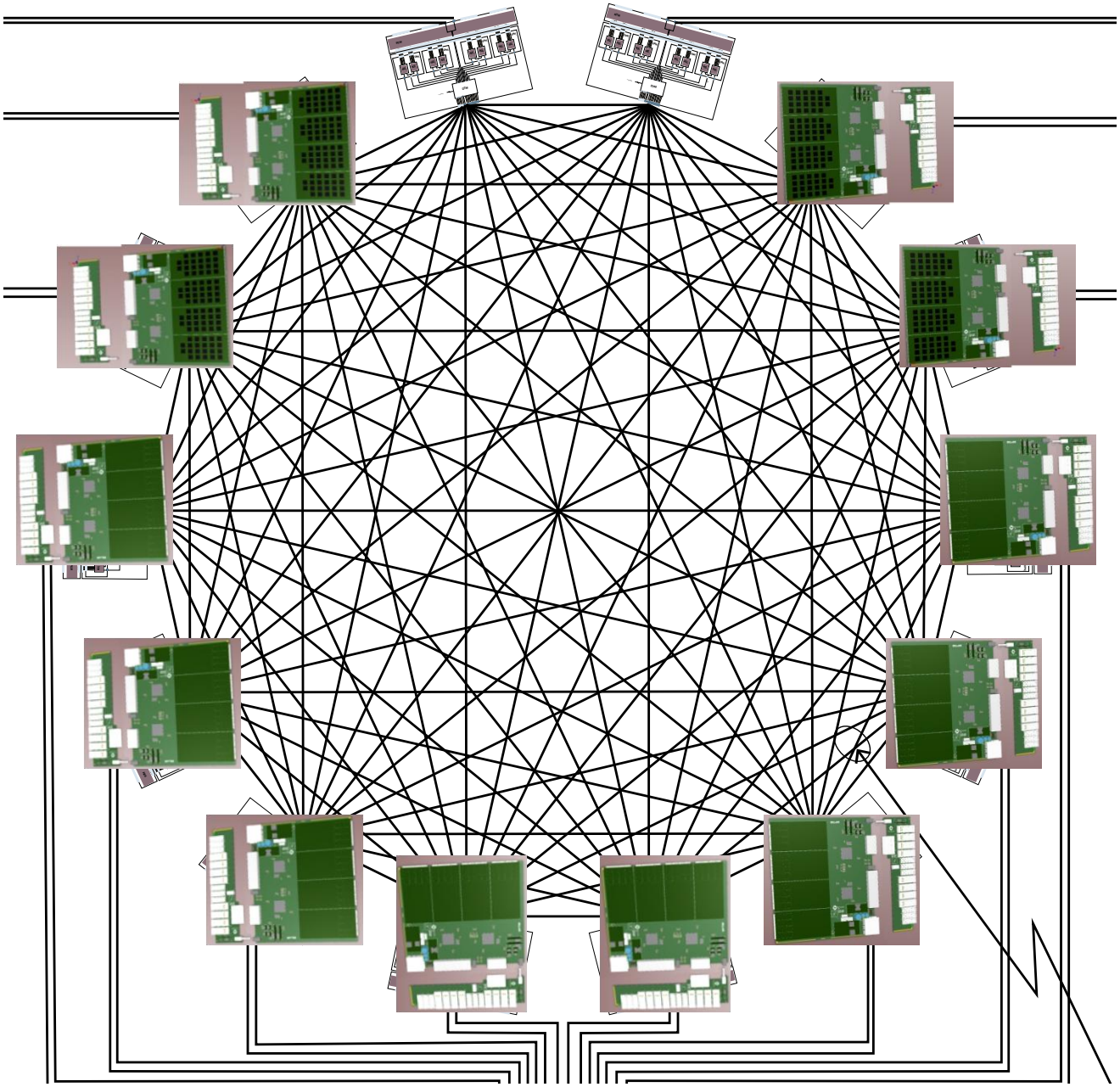
Two high schoolers having fun

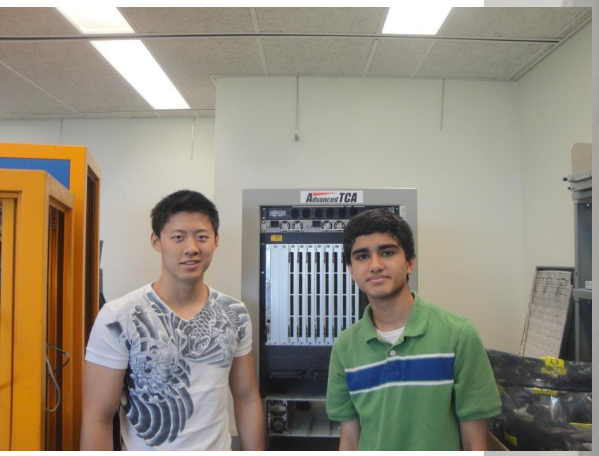


Testing Prototype boards









Rear Transition Module (RTM)

Full Mesh Backplane

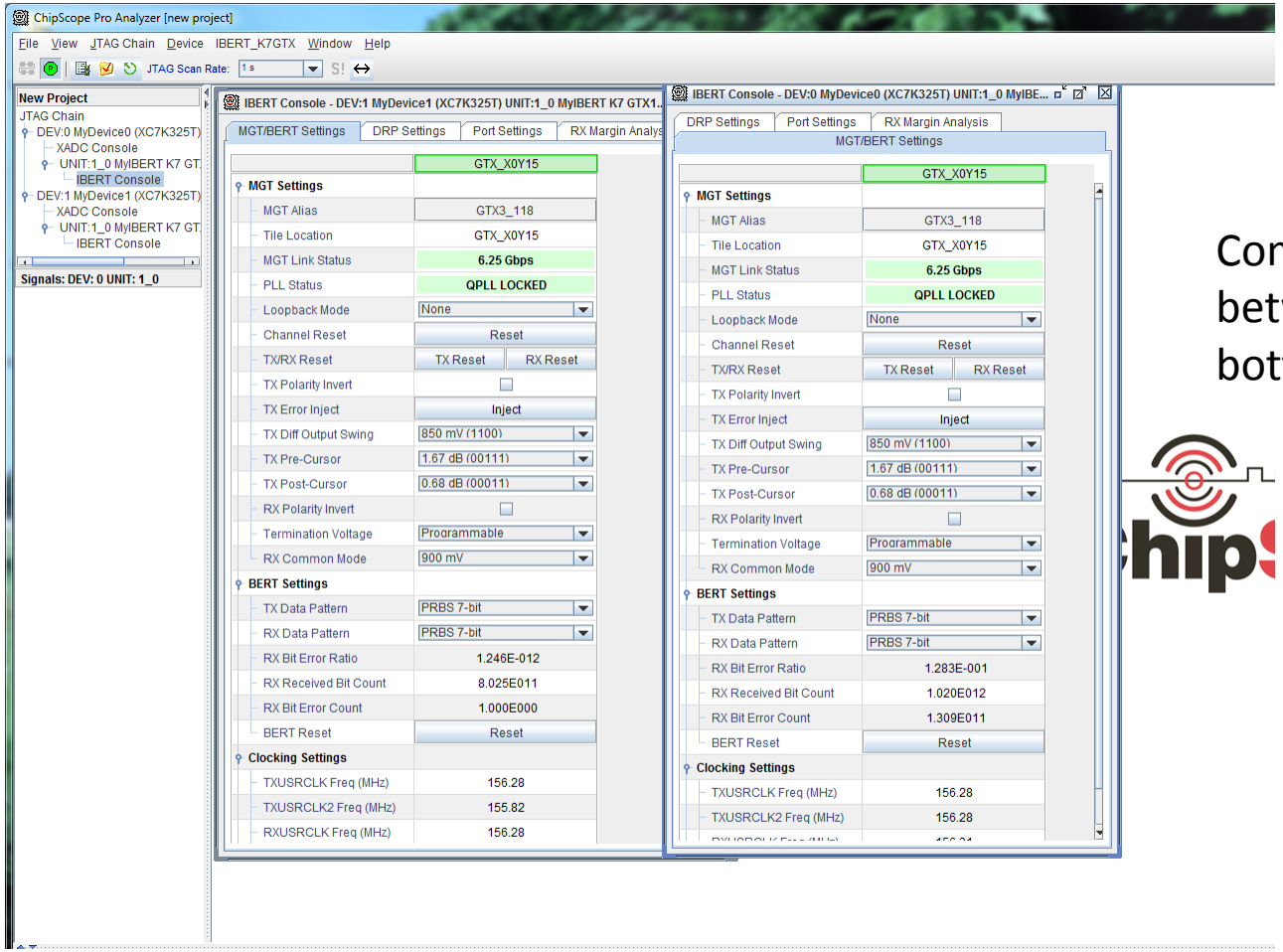
Table 6-11 Full Mesh Backplane routing assignments

	Logical Slot #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Connect or	Channel #																
P20	15	16-1	16-2	16-3	16-4	16-5	16-6	16-7	16-8	16-9	16-10	16-11	16-12	16-13	16-14	16-15	15-15
P20	14	15-1	15-2	15-3	15-4	15-5	15-6	15-7	15-8	15-9	15-10	15-11	15-12	15-13	15-14	14-14	14-15
P20	13	14-1	14-2	14-3	14-4	14-5	14-6	14-7	14-8	14-9	14-10	14-11	14-12	14-13	13-13	13-14	13-15
P21	12	13-1	13-2	13-3	13-4	13-5	13-6	13-7	13-8	13-9	13-10	13-11	13-12	12-12	12-13	12-14	12-15
P21	11	12-1	12-2	12-3	12-4	12-5	12-6	12-7	12-8	12-9	12-10	12-11	11-11	11-12	11-13	11-14	11-15
P21	10	11-1	11-2	11-3	11-4	11-5	11-6	11-7	11-8	11-9	11-10	10-10	10-11	10-12	10-13	10-14	10-15
P21	9	10-1	10-2	10-3	10-4	10-5	10-6	10-7	10-8	10-9	9-9	9-10	9-11	9-12	9-13	9-14	9-15
P21	8	9-1	9-2	9-3	9-4	9-5	9-6	9-7	9-8	8-8	8-9	8-10	8-11	8-12	8-13	8-14	8-15
P22	7	8-1	8-2	8-3	8-4	8-5	8-6	8-7	7-7	7-8	7-9	7-10	7-11	7-12	7-13	7-14	7-15
P22	6	7-1	7-2	7-3	7-4	7-5	7-6	6-6	6-7	6-8	6-9	6-10	6-11	6-12	6-13	6-14	6-15
P22	5	6-1	6-2	6-3	6-4	6-5	5-5	5-6	5-7	5-8	5-9	5-					
P22	4	5-1	5-2	5-3	5-4	4-4	4-5	4-6	4-7	4-8	4-9	4-					
P22	3	4-1	4-2	4-3	3-3	3-4	3-5	3-6	3-7	3-8	3-9	3-					
P23	2	3-1	3-2	2-2	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-					
P23	1	2-1	1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-					

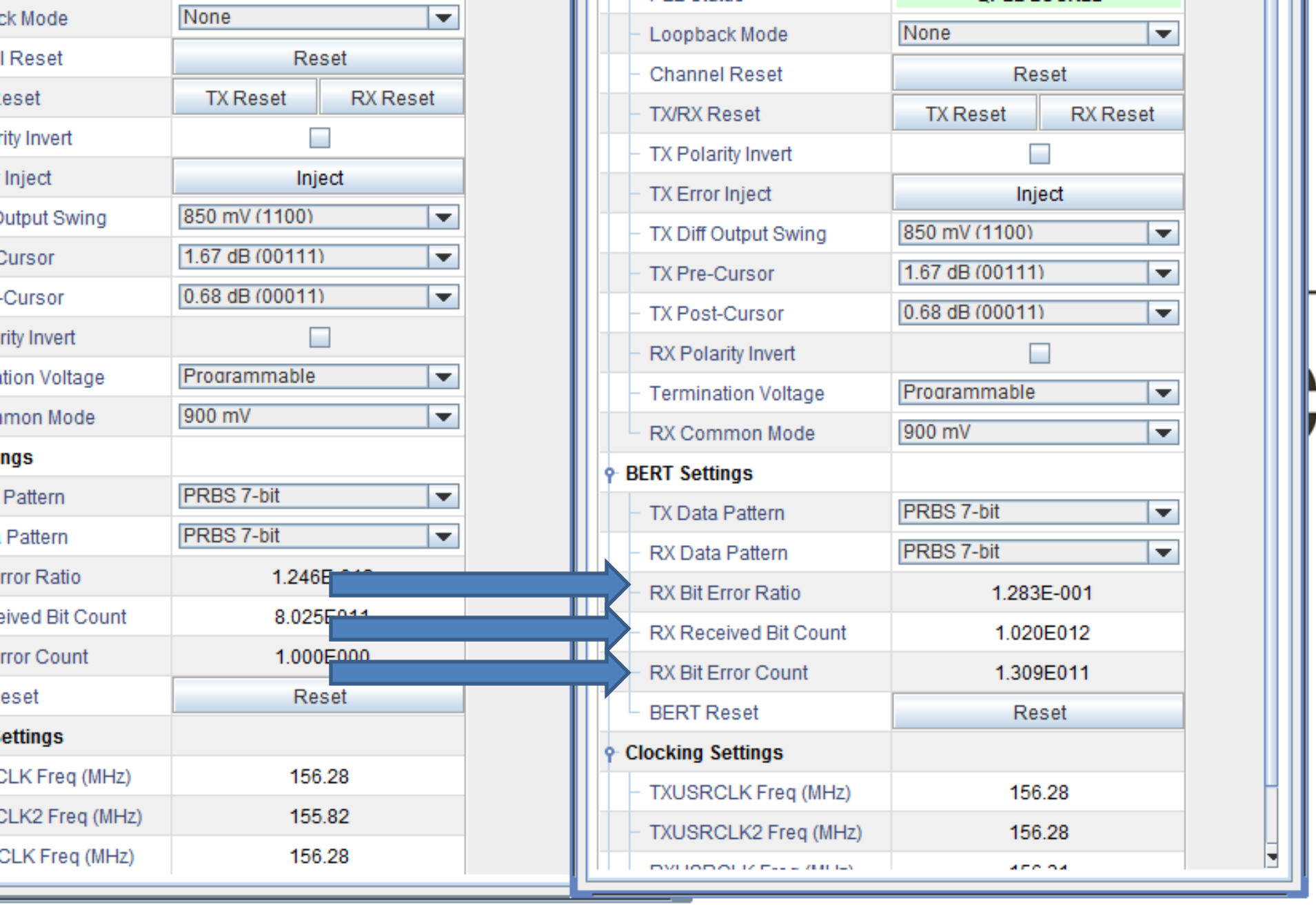
Prototype Board in Crate

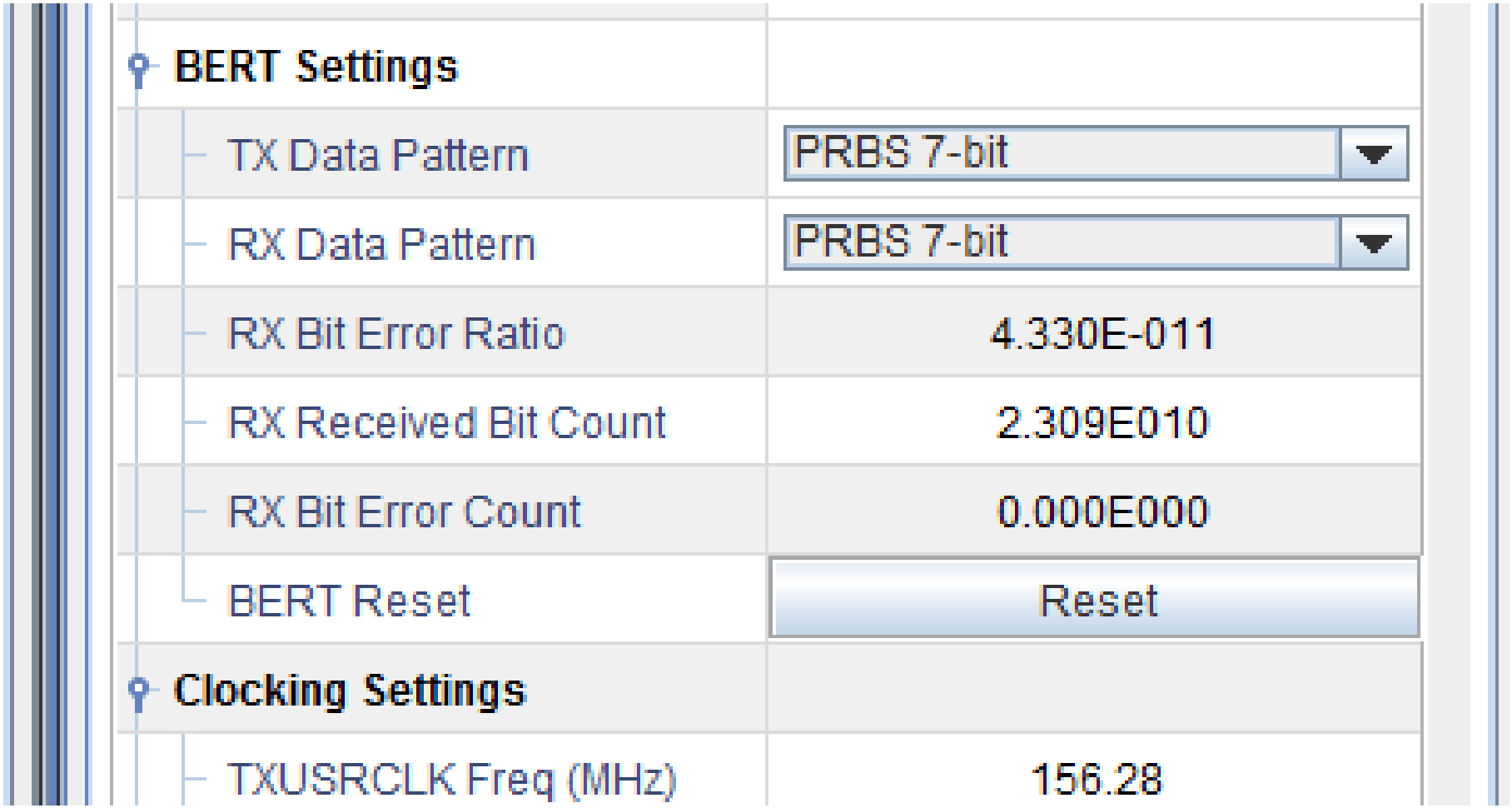
Board has been inserted and powered on

Test for local bus



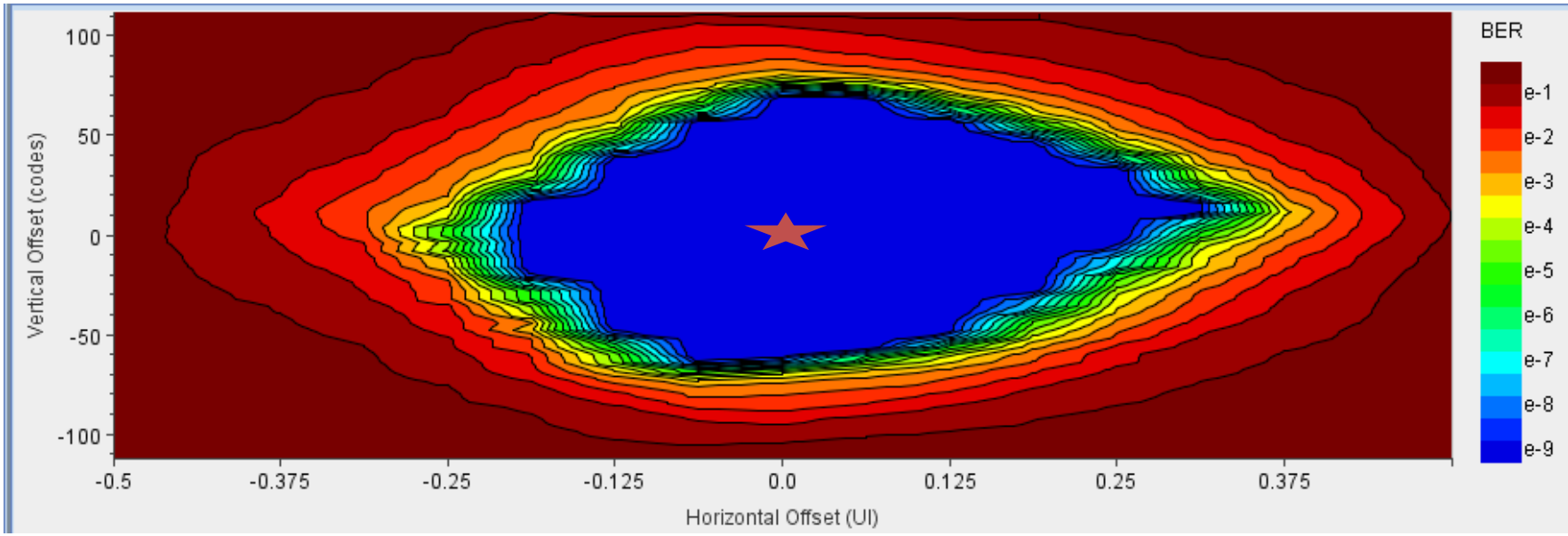
Communication between top and bottom FPGAs


None
Reset
TX Reset
RX Reset
Inject
850 mV (1100)
1.67 dB (00111)
0.68 dB (00011)
Programmable
900 mV
PRBS 7-bit
PRBS 7-bit
1.246E
8.025E011
1.000E000
Reset
156.28
155.82
156.28
Loopback Mode
None
Channel Reset
Reset
TX/RX Reset
TX Reset
RX Reset
TX Polarity Invert
TX Error Inject
Inject
TX Diff Output Swing
850 mV (1100)
TX Pre-Cursor
1.67 dB (00111)
TX Post-Cursor
0.68 dB (00011)
RX Polarity Invert
Termination Voltage
Programmable
RX Common Mode
900 mV
BERT Settings
TX Data Pattern
PRBS 7-bit
RX Data Pattern
PRBS 7-bit
RX Bit Error Ratio
1.283E-001
RX Received Bit Count
1.020E012
RX Bit Error Count
1.309E011
BERT Reset
Reset
Clocking Settings
TXUSRCLK Freq (MHz)
156.28
TXUSRCLK2 Freq (MHz)
156.28


BERT Settings
TX Data Pattern
PRBS 7-bit
RX Data Pattern
PRBS 7-bit
RX Bit Error Ratio
4.330E-011
RX Received Bit Count
2.309E010
RX Bit Error Count
0.000E000
BERT Reset
Reset
Clocking Settings
TXUSRCLK Freq (MHz)
156.28

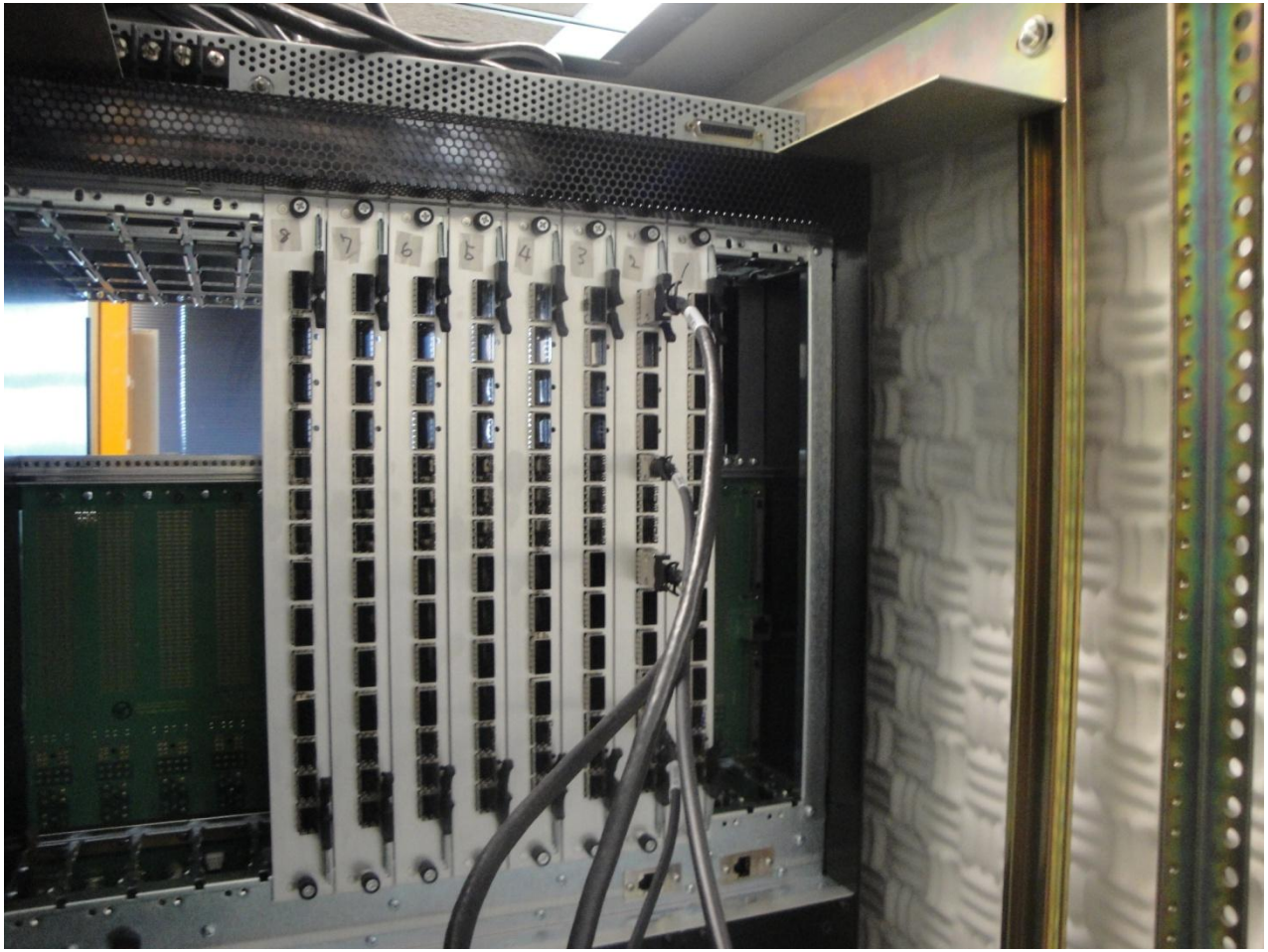
2D Eye Scan

Voltage (mV)

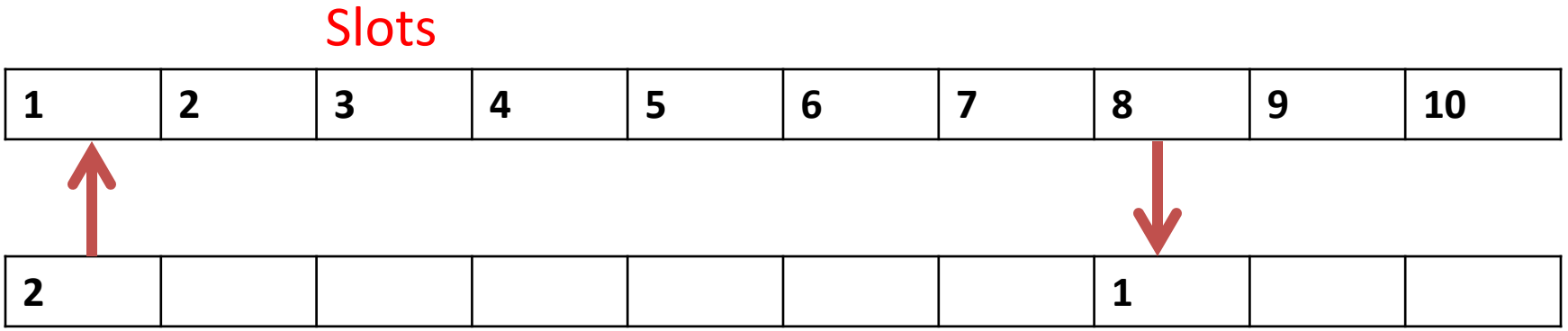


Sound (dB)

Rear Transition Module (RTM)



Systematic Problem Solving

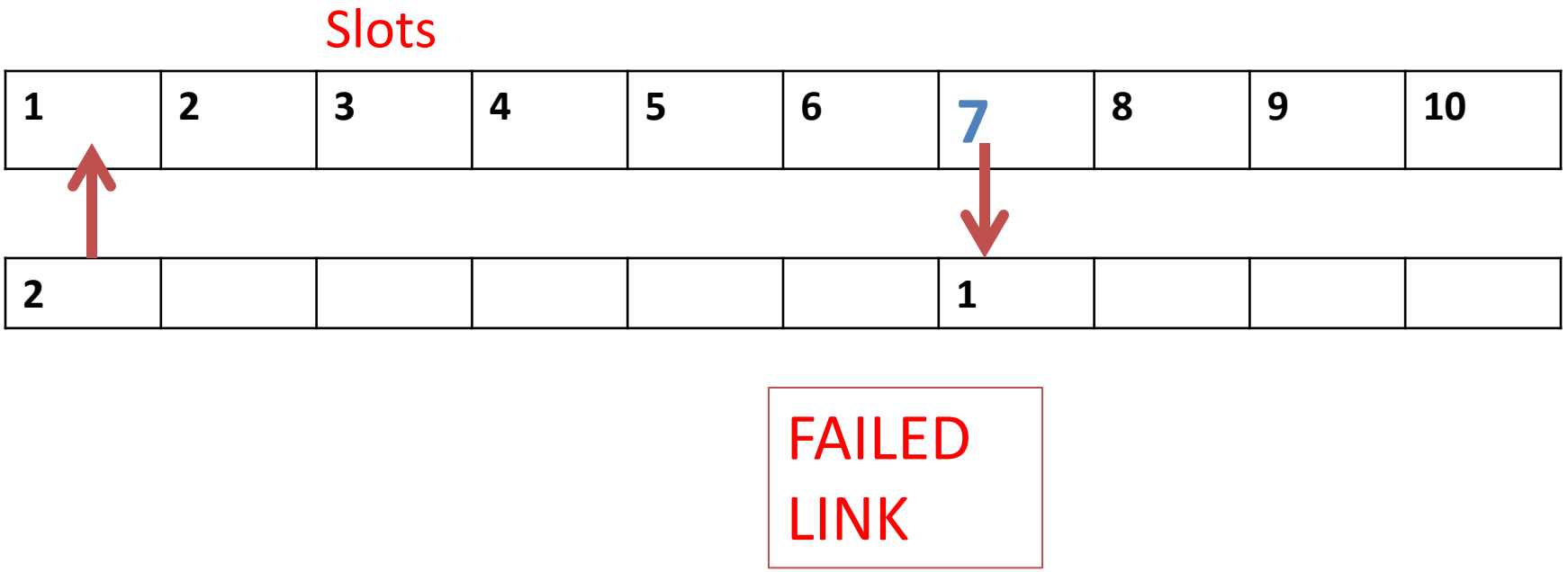


FAILED LINK

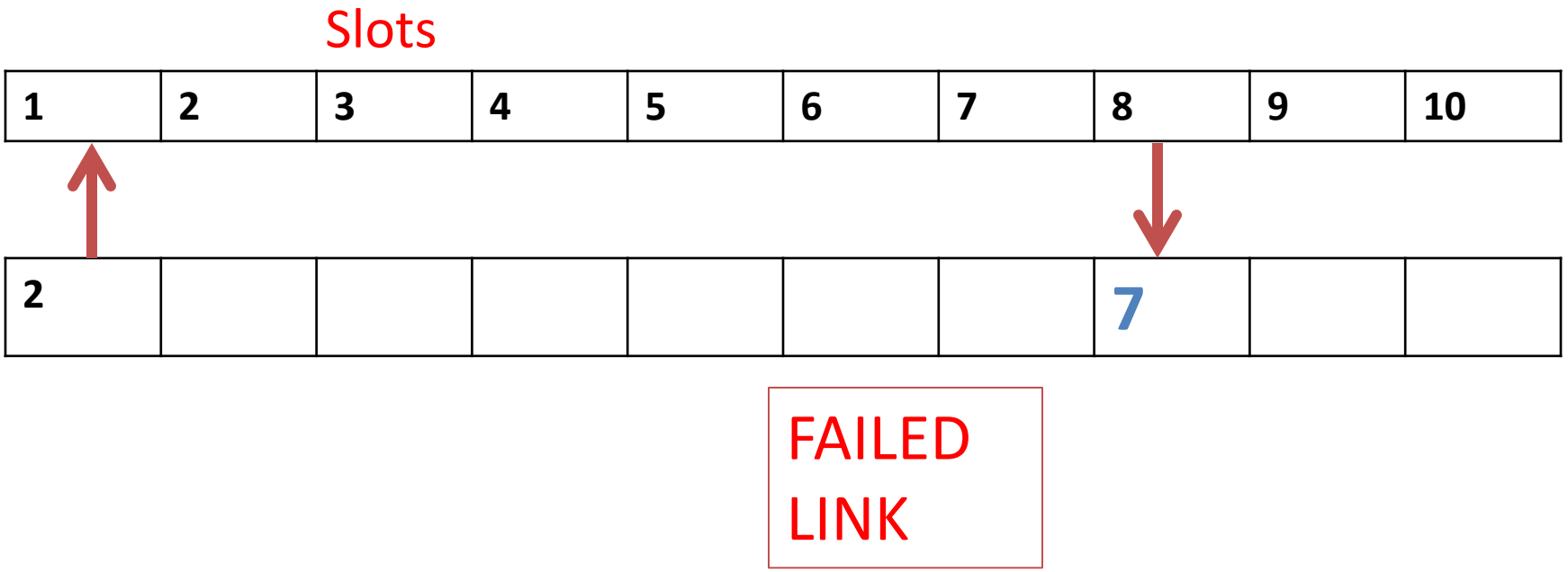
Candidates for causing problem:

- Pins in ATCA Crate (Slot 1 and 8)
- Problems in Board 2 and 1 in the lines required for communication

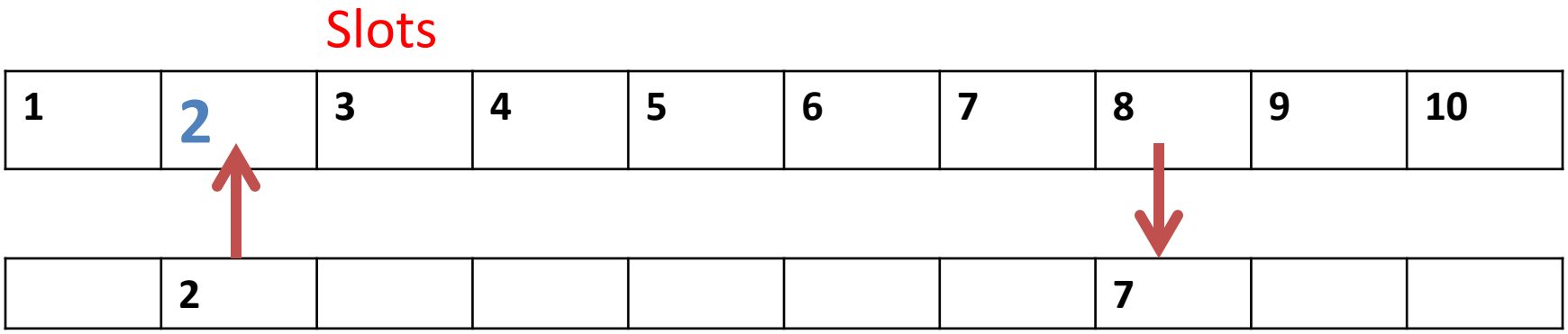
Changing Slot 8 to Slot 7



Changing board 1 to 7



Changing Slot 1 to 2



Hypothesis:
Damaged or Missing pins exist in Board 2 in channel 8

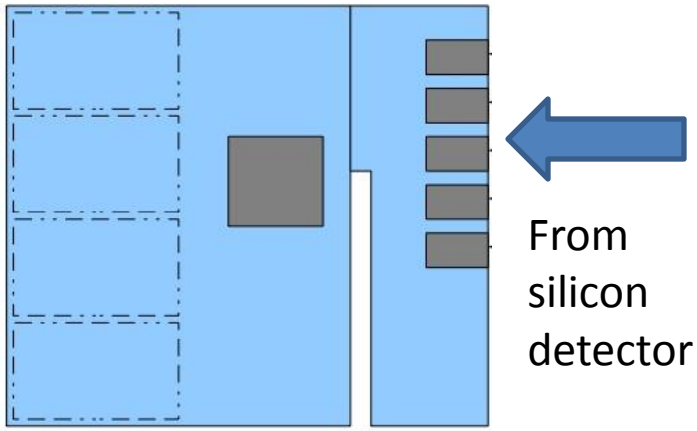
FAILED LINK

Testing Completed

- The 8 boards have been checked for
  - Local bus (communication between FPGAs) successful for all boards
  - RTM (6 of 8 boards – no errors, 2 boards had problematic channels)
  - ATCA Backplane (3 board tested, 1 problematic channel discovered)

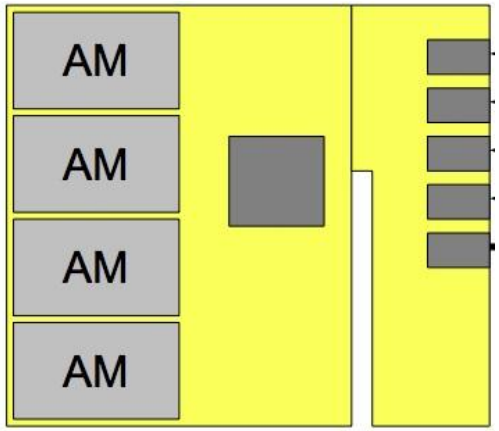
Crate/board level

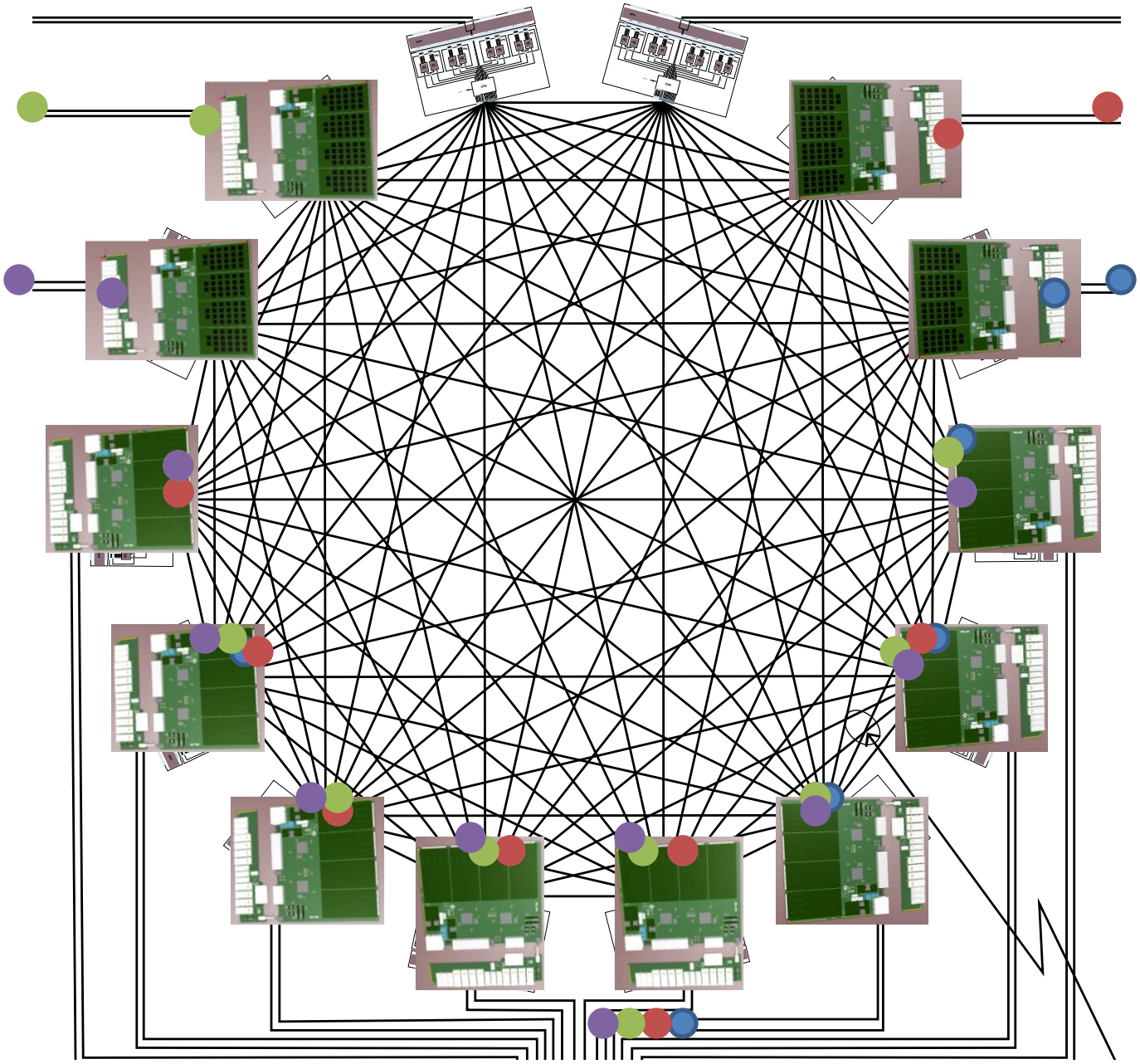
Input board x 8

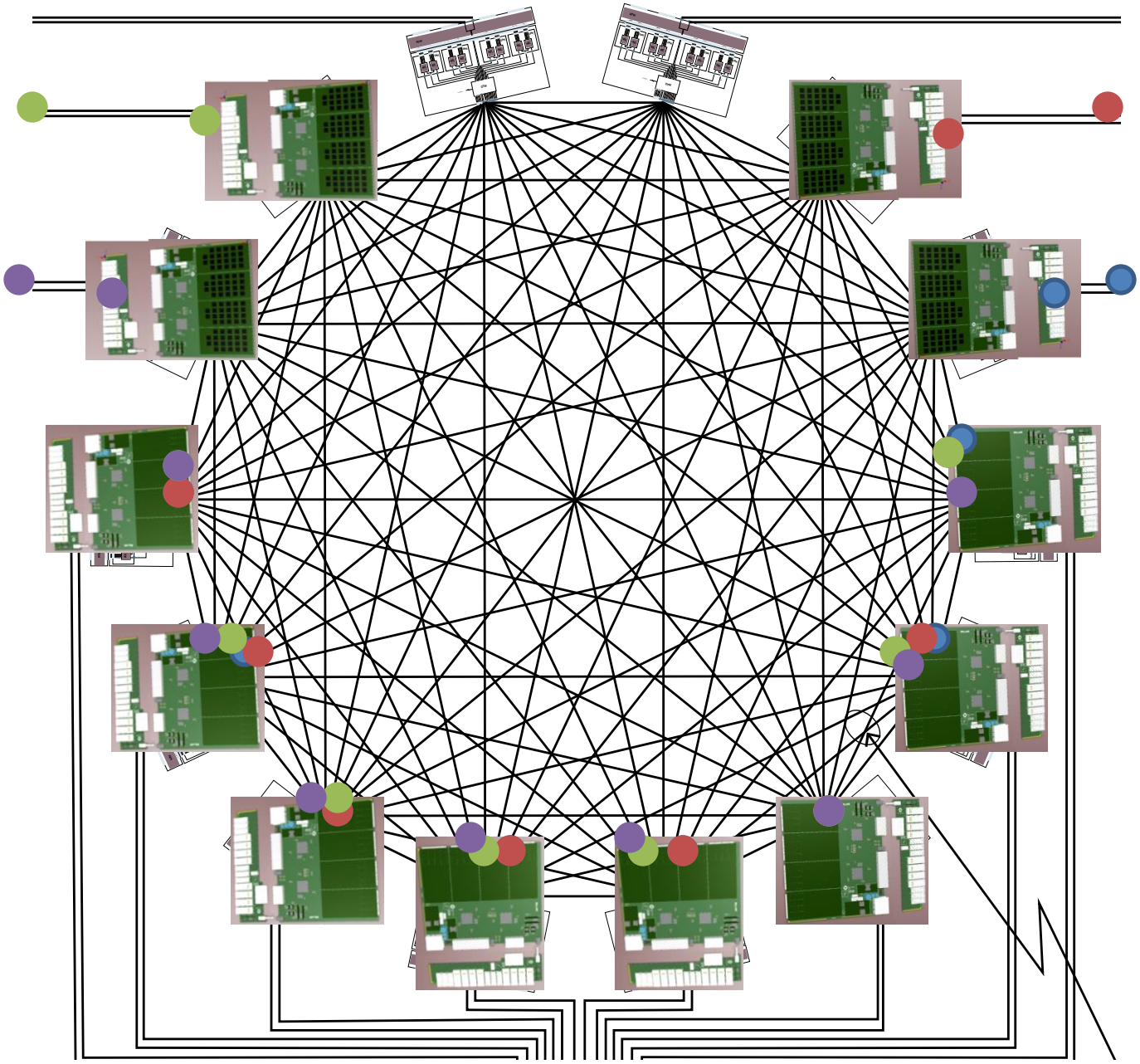


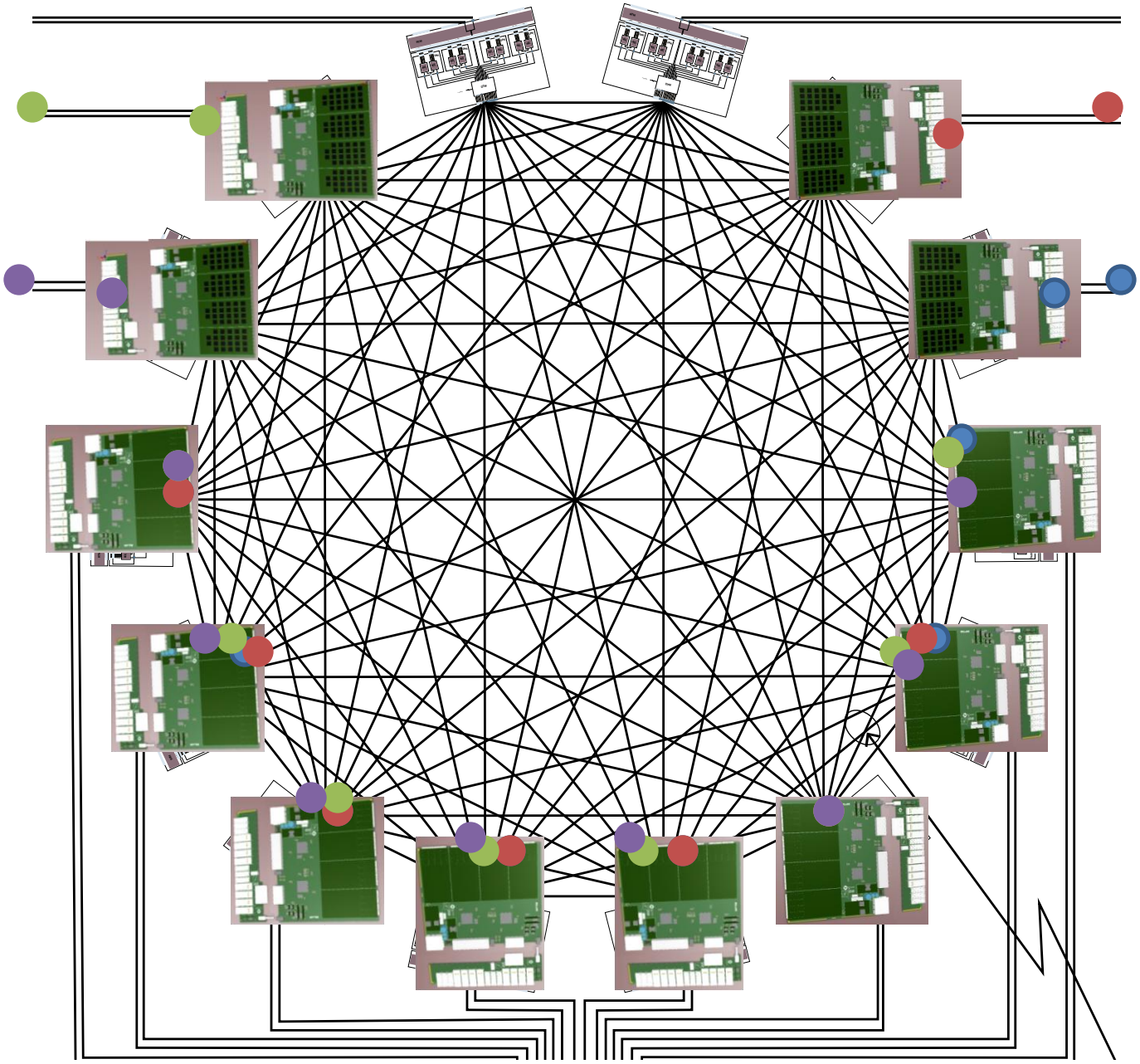
From silicon detector

AM board x 4

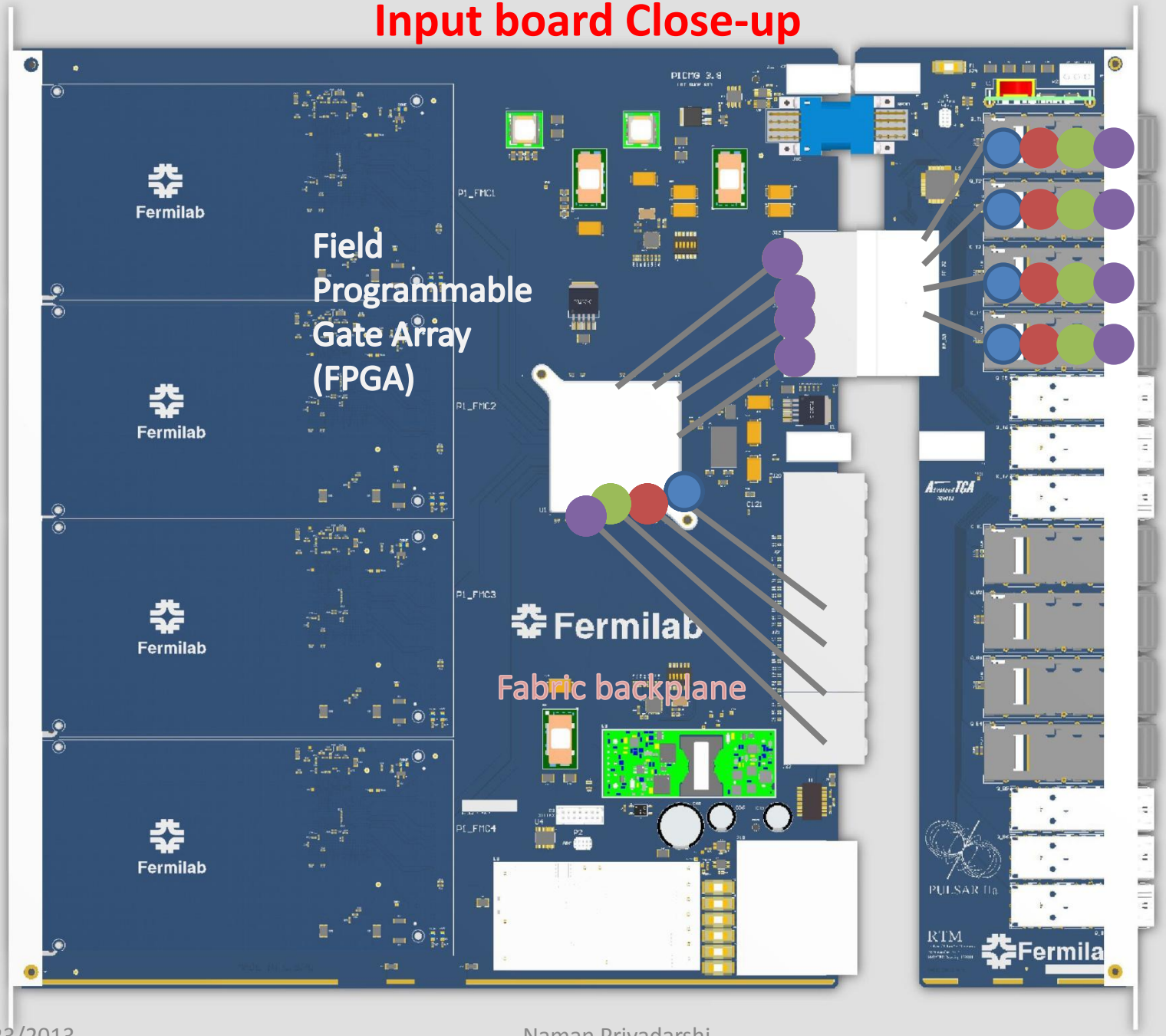




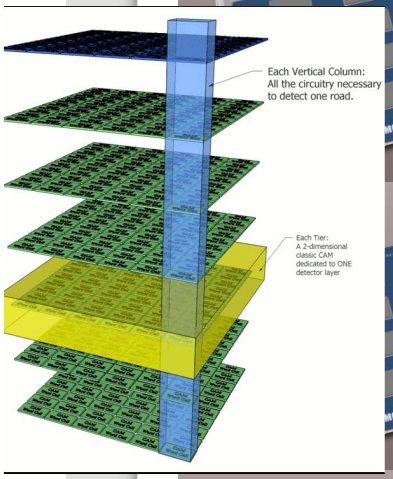




Input board Close-up



AM board Close-up

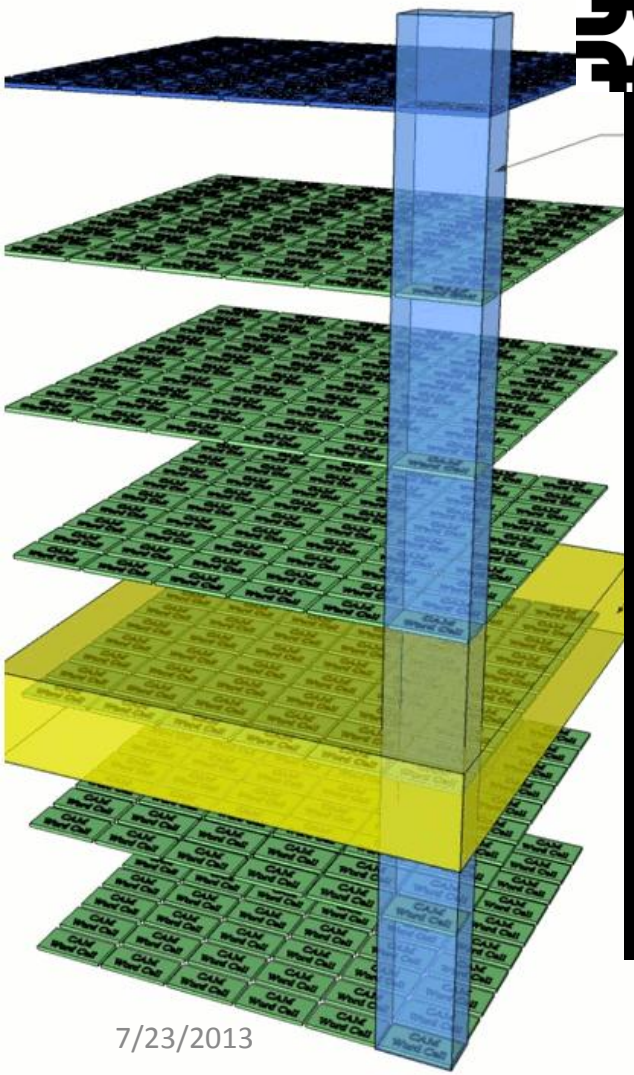


"A New Concept of Vertically Integrated Pattern Recognition Associative Memory"

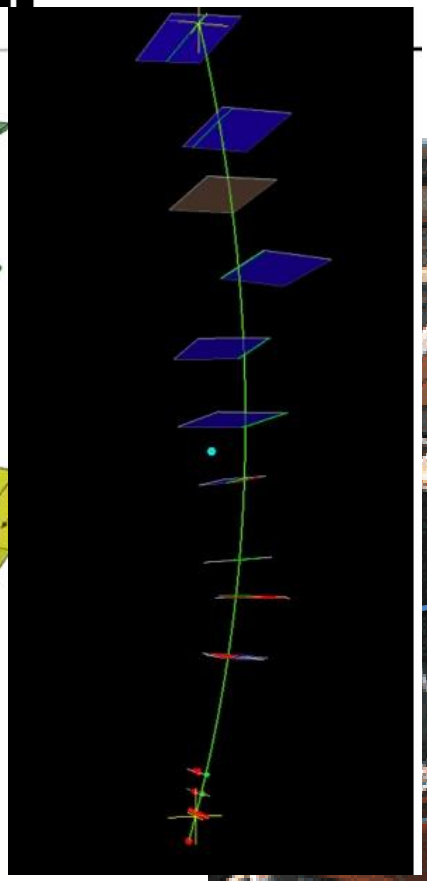
TIPP 2011 Proceedings

http://www.sciencedirect.com/science/article/pii/S1875389212019165

fired road

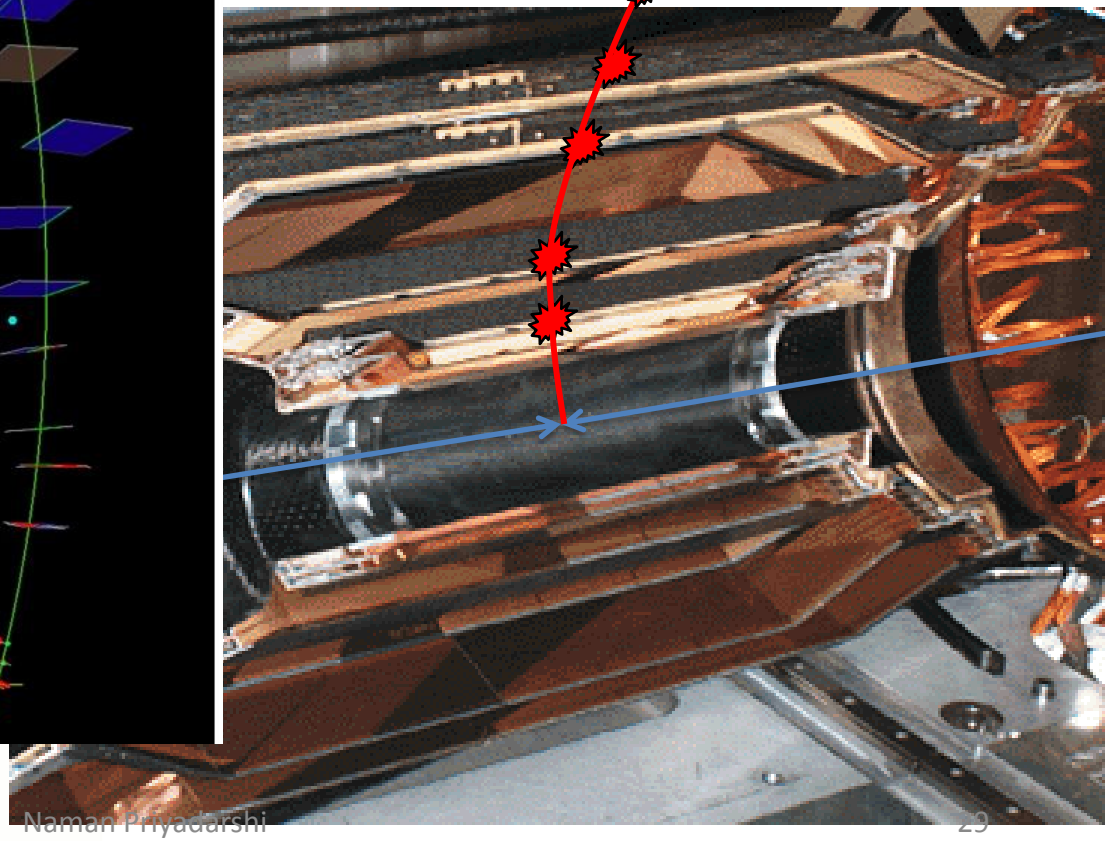


Fermilab



Pattern recognition for tracking is naturally a task in 3D

track



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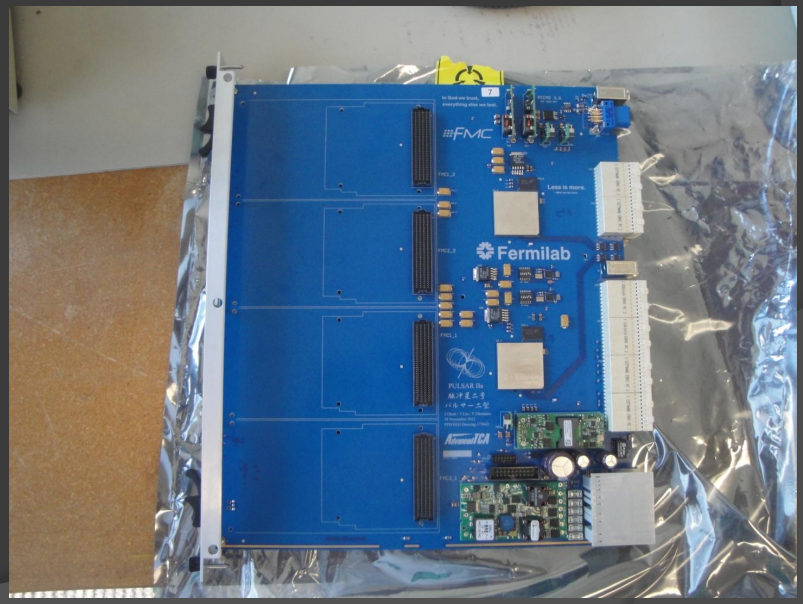
HL-LHC L1 Tracking Trigger is High Performance Computing
(Non-von Neumann approach)
Low Latency and Real Time

Summary

- Level 1 tracking Trigger will be necessary for future LHC experiments during higher luminosity
- Goal of the new system is to go far beyond current high performance computing with near zero latency
- Opportunities to use 3D IC in future
  - Smart-phones
  - High-performance Digital Video
  - Wireless Connectivity



My Learning Experience at Fermilab

- A newfound understanding and appreciation of hardware by understanding this system
- Opportunity to work with scientists on cutting edge parallel processing technology
- Chance to learn and practice a systematic way to solving problems