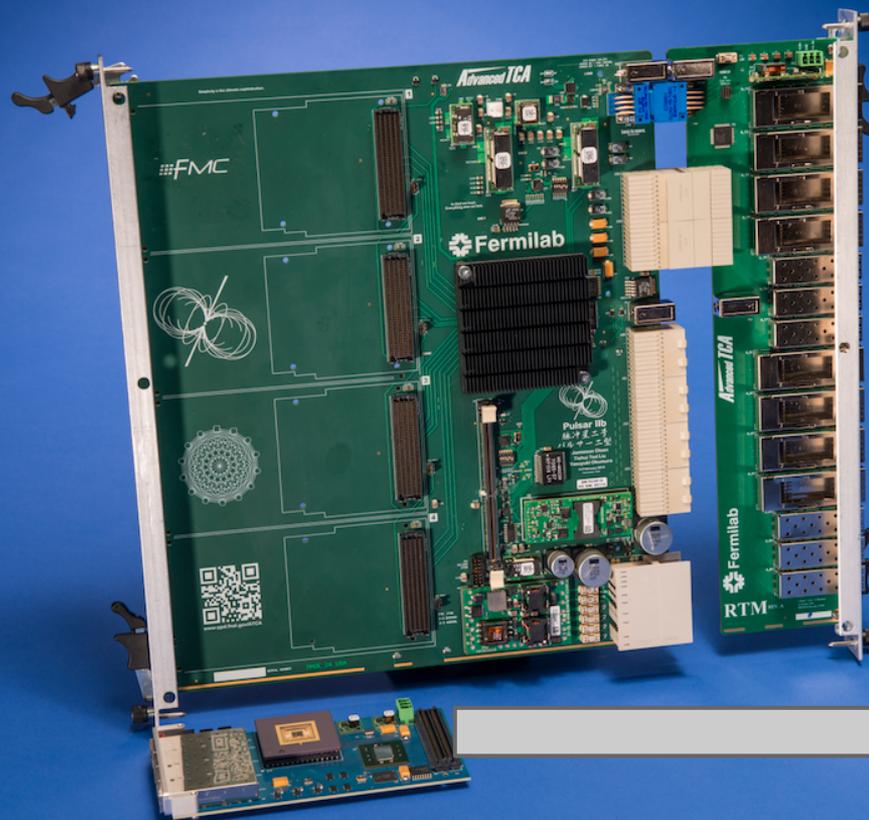


# Pulsar II & VIPRAM Chip



**Lauren Craig**  
**QuarkNet Intern**

# Topics of Discussion

- Short video on technology of Pulsar II and VIPRAM Chip
- High Luminosity LHC Tracking Trigger Challenges
- Fermilab Tracking Trigger R&D program: Pulsar II and VIPRAM Chip Technology
- Performance study of the VIPRAM prototype chips by pushing beyond its limits
- Acknowledgements

Short Video  
on  
Technology  
of Pulsar II  
and VIPRAM





# Tracking Trigger at LHC

- LHC will need to upgrade by the year 2020 to the High Luminosity LHC. This will make the particle accelerator more efficient for more discoveries.
- LHC needs to increase rate of collisions by a factor of ten.
- There will be a need for a silicon detector based tracking trigger with fast pattern recognition.

# High Luminosity LHC Tracking Trigger Challenges

- Two main challenges
  - To be able to handle huge volume of data with more than 100 Tbps transfer bandwidth over 15,000 fibers.
  - To have extremely short processing latency (few microseconds) to reconstruct charged particles from collisions.
- Over the past few years, Fermilab has created a system (based on Pulsar II and VIPRAM) to fill this pattern recognition need for the future.
- Pulsar II and VIPRAM technologies will be key to interpret data and find interesting events from particle collisions without being overwhelmed by a large background of information.

# Pulsar II System

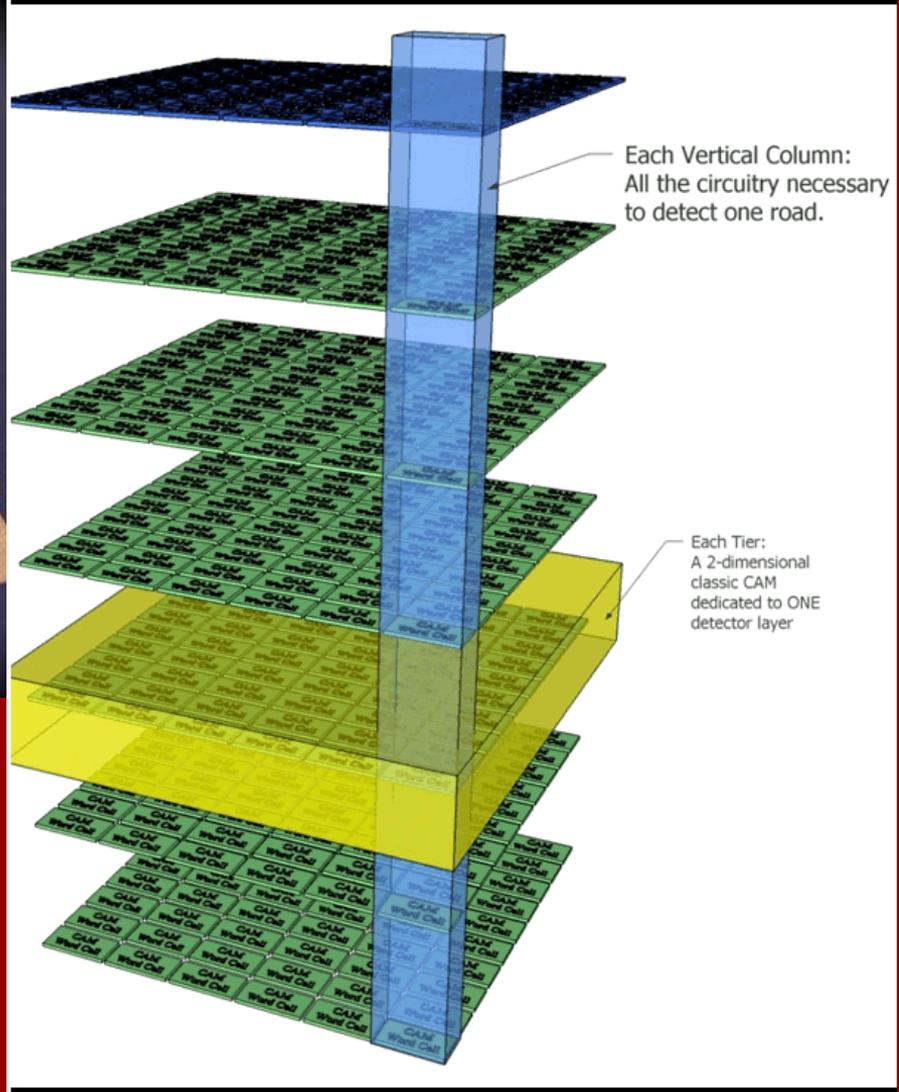
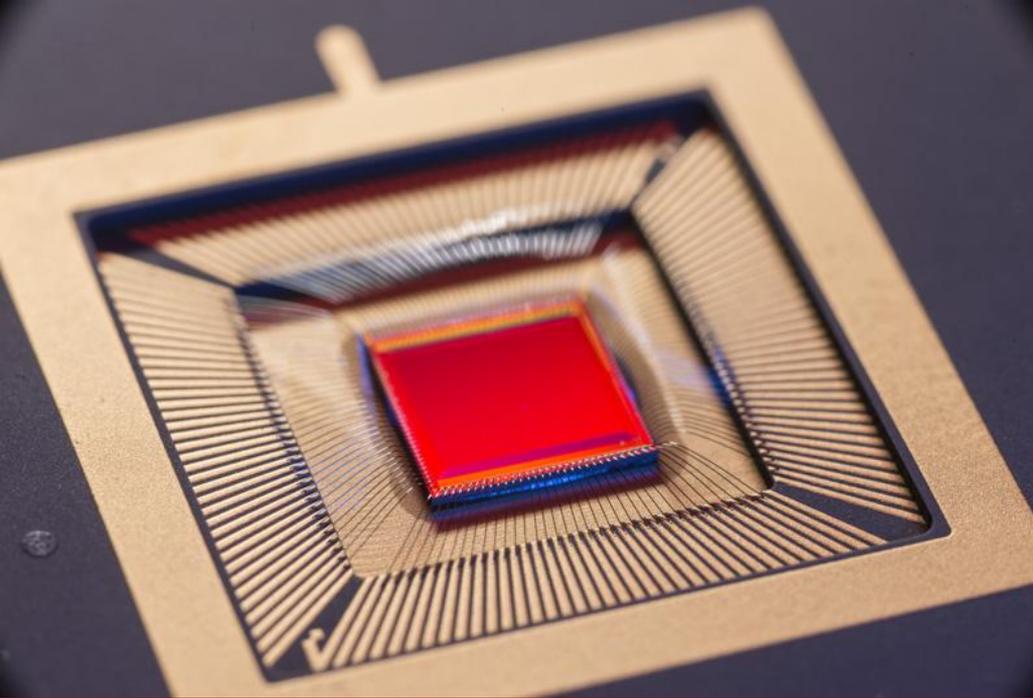


# About Pulsar II

- Pulsar II and VIPRAM can be used to form a general purpose high speed pattern recognition system which can be used for many purposes within and beyond High Energy Physics.
- The processing will be in real-time with very low latency which is key to successfully interpreting large quantities of data at the HL LHC.
- Pulsar II is based on ATCA technology standard (Advanced Telecommunication Computing Architecture).

# About VIPRAM

- Vertically Integrated Pattern Recognition Associative Memory.
- VIPRAM is a new 3D associative memory implementation that is denser and faster than other conventional 2D associative memory implementations.
- VIPRAM layers are composed of CAM Cells .
- CAM = Content Addressable Memory.
- Each CAM Cell can have preloaded information to be matched to incoming data “on the fly”.



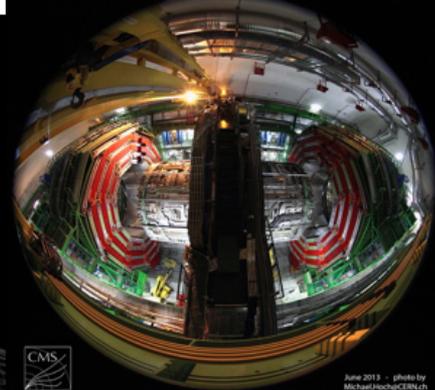
**When data enters VIPRAM and finds a match to a preloaded pattern on the CAM Cells, a road is made.**

# Flow of data from LHC

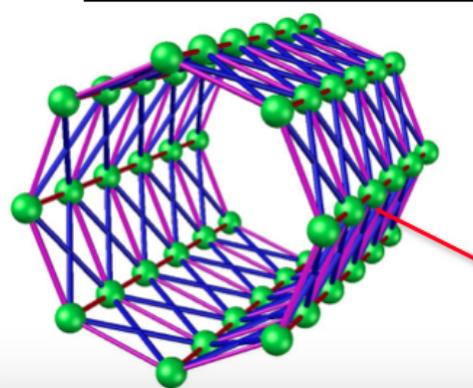
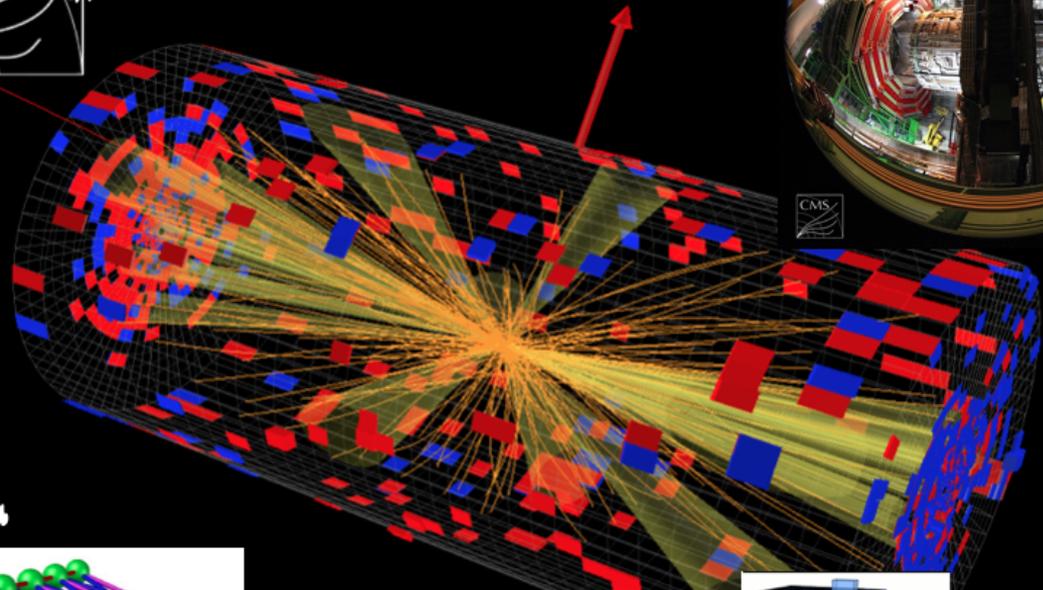
- CMS silicon based detector will record the hits produced by the charged particles coming out from proton collisions.
- The data (hits, ~100Tbps) will then be sent from the LHC detector to the Pulsar-like system where it will be compared to patterns preloaded by users on the fly. Tracks will be found this way within a few microseconds after collision.



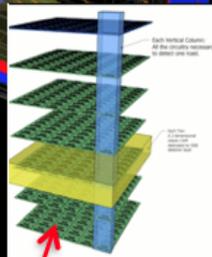
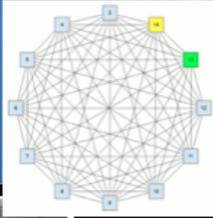
CMS Experiment at LHC, CERN  
Data recorded: Thu Apr 5 01:18:00 2012 CEST  
Run/Event: 190389 / 107592030  
Lumi section: 138



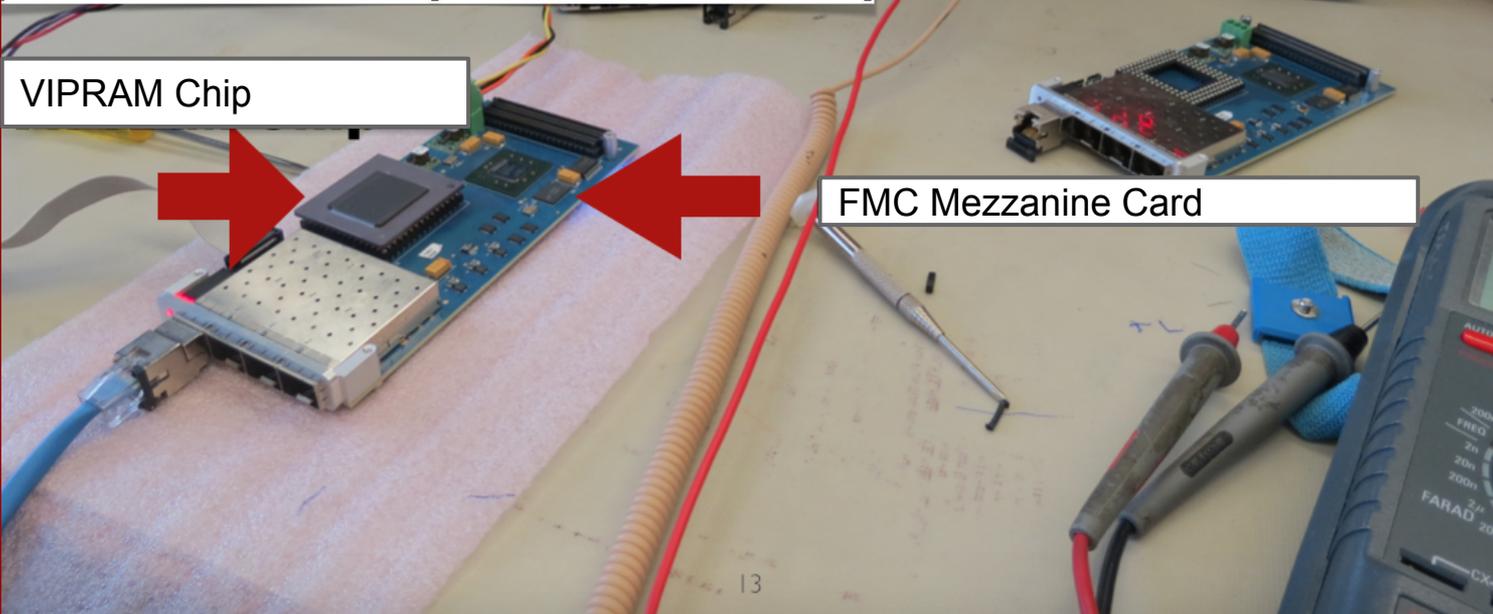
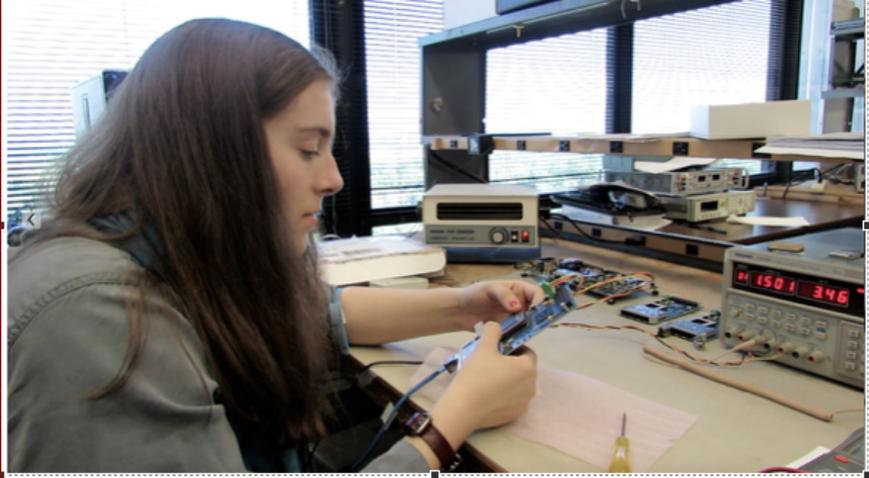
June 2013 - photo by Michael Hochberg/CERN/CH



CMS Tracking Trigger Towers



AM or other track finding approaches implemented on mezzanine (PR engine)



VIPRAM Chip

FMC Mezzanine Card

## VIPRAM Project Status Summary

### *The past: with steady progress*

Initial concept developed: ~2010

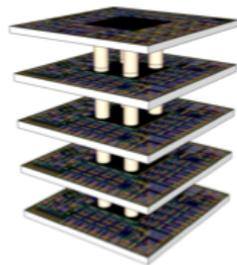
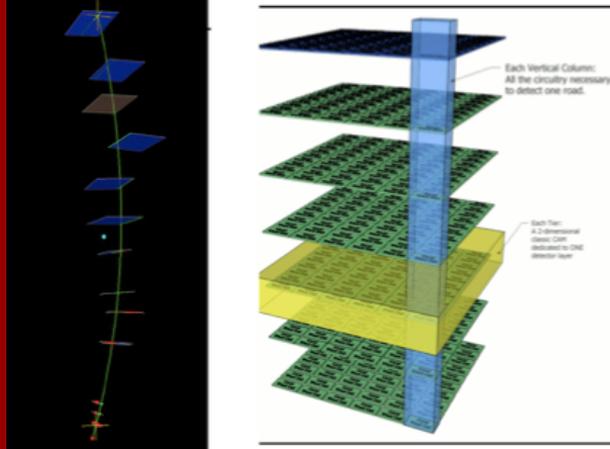
VIPRAM concept paper: 2011

CDRD award: 2012

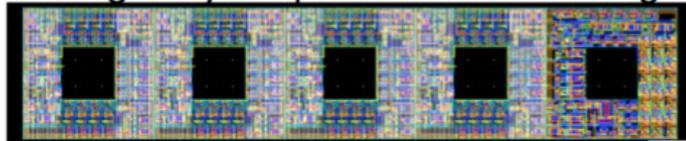
First 2D Design submission: 2013

**First ProtoVIPRAM00 chip successfully tested: 2014**

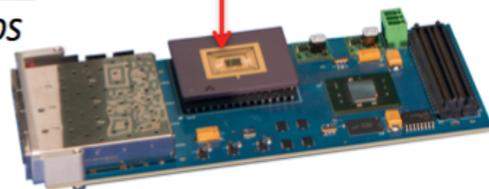
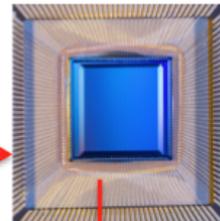
→ **Design building blocks are ready for 3D stacking**



2D design fully compatible with 3D stacking



CAM cell size: 25  $\mu\text{m}$  x 25  $\mu\text{m}$ , @ 130nm GF CMOS



### *The present and future:*

**The actual 3D design (protoVIPRAM01) ready: ~ end of 2014**

**A 2-tier design for CMS L1 tracking trigger (protoVIPRAM02): 2014-2015**

Have both designs ready for submission: 2015

# Performance studies on VIPRAM chips

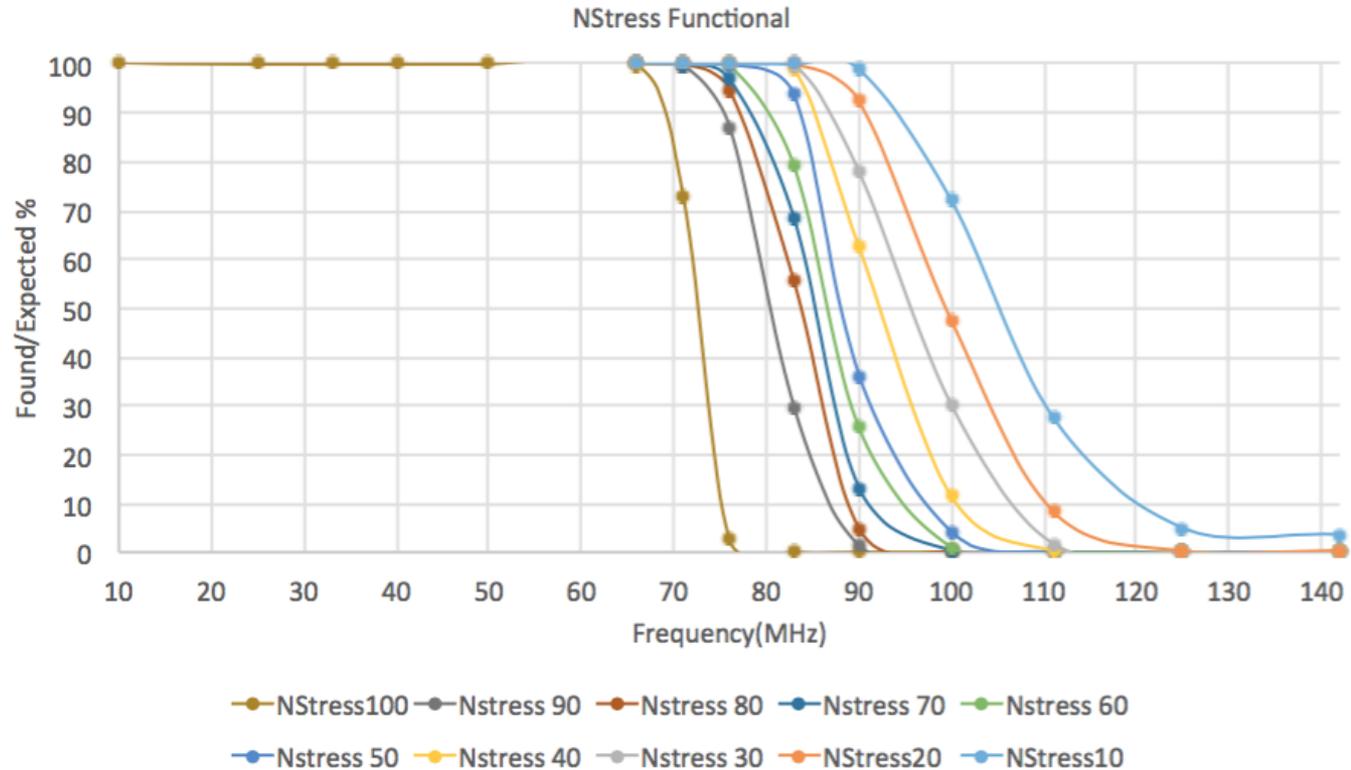
- Tests performed on VIPRAM chips demonstrate the ability of the chips to successfully process and interpret preloaded patterns at given speeds.
- VIPRAM chips have been extensively tested using HL-LHC CMS simulation data for the tracking trigger applications, and works well as designed (up to 111 MHz).
- Stress tests push VIPRAM chips beyond its design limit (for LHC needs) to see what it can really handle in extreme conditions beyond LHC.
- Stress tests involves changing the speed of operation as well as the percentage of matched CAM cells.

# Stress testing VIPRAM

- Match % represents how successfully the VIPRAM Chip matches the data with preloaded patterns.
- NStress % represents the percentage of matches for each test
- I tested 10 different NStress levels from 10-100 (increments of 10) with twelve operating frequencies (10, 25, 33, 50, 66, 71, 76, 83, 90, 100, 111, 125).
- All of these tests were done on a series of VIPRAM Chips and on FMC Mezzanine Card 2.



# Functional Analysis Stress Test: Match Found/Expected



# New Learning Experiences At QuarkNet

- Fundamental science research and applying new knowledge to hands on experience.
- Advanced technology- would not experience at home or school.
- Python and VHDL software language.
- Learned how to test modern electronics
- VIPRAM and Pulsar II technology.
- LHC Detector and tracking trigger knowledge.
- Jargon for computer hardware language.

# Acknowledgements

## Fermilab

- Dr. Ted Liu-Mentor
- Dr. Nhan Tran
- Dr. Sergo Jindariani
- Zijun Xu
- Dr. Chris Stoughton
- George Dzuricsko
- Ben Sawyer
- QuarkNet Interns