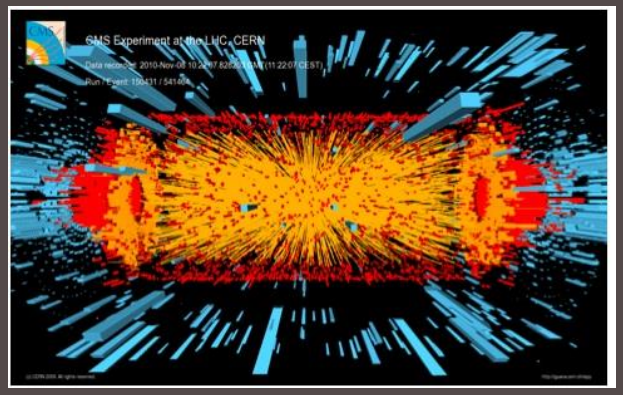
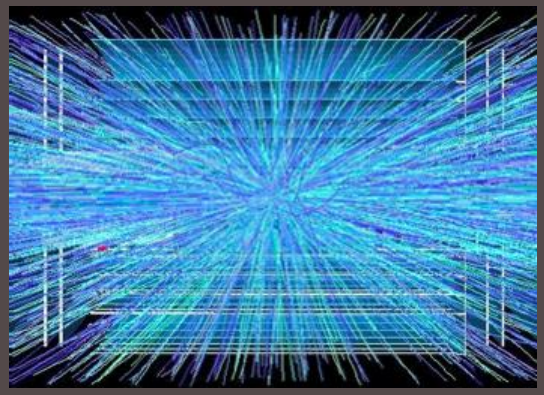
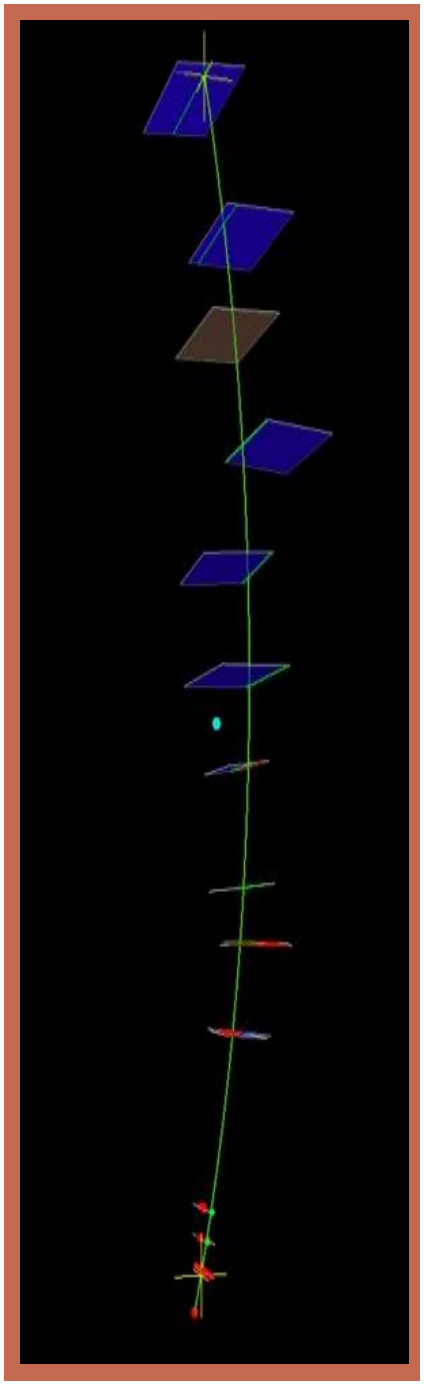




PERFORMANCE STUDIES FOR HIGH SPEED DATA COMMUNICATION FOR CMS TRACKING TRIGGER

Stacy Wang
Montville High School
July 30, 2014
Dr. Ted Liu
Quarknet

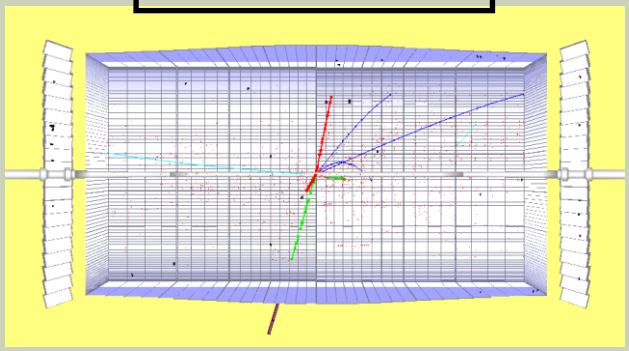
Fermilab



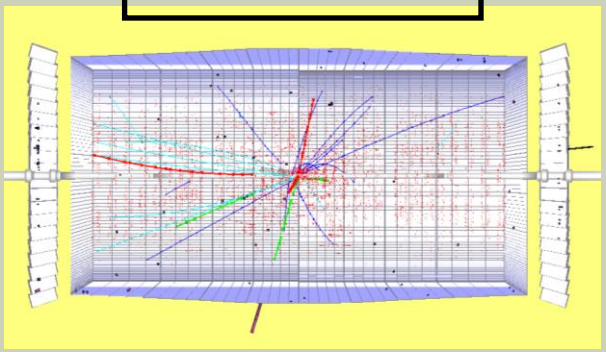
PILE UP V LUMINOSITY

CMS Occupancy v LHC Luminosity

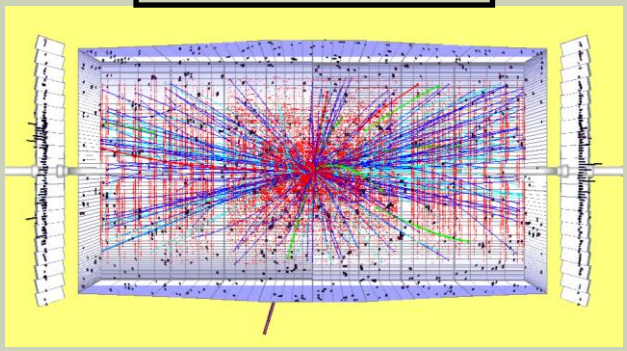
10^{32} $cm^{-2}s^{-1}$



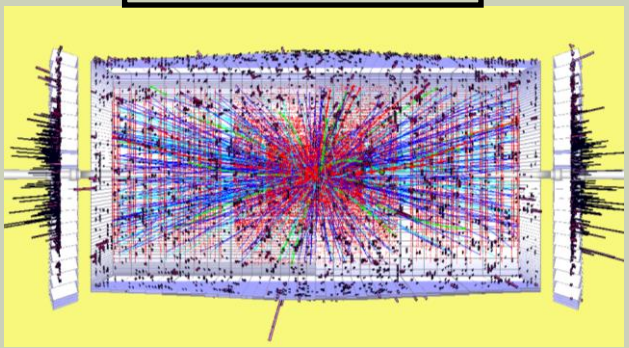
10^{33} $cm^{-2}s^{-1}$



10^{34} $cm^{-2}s^{-1}$



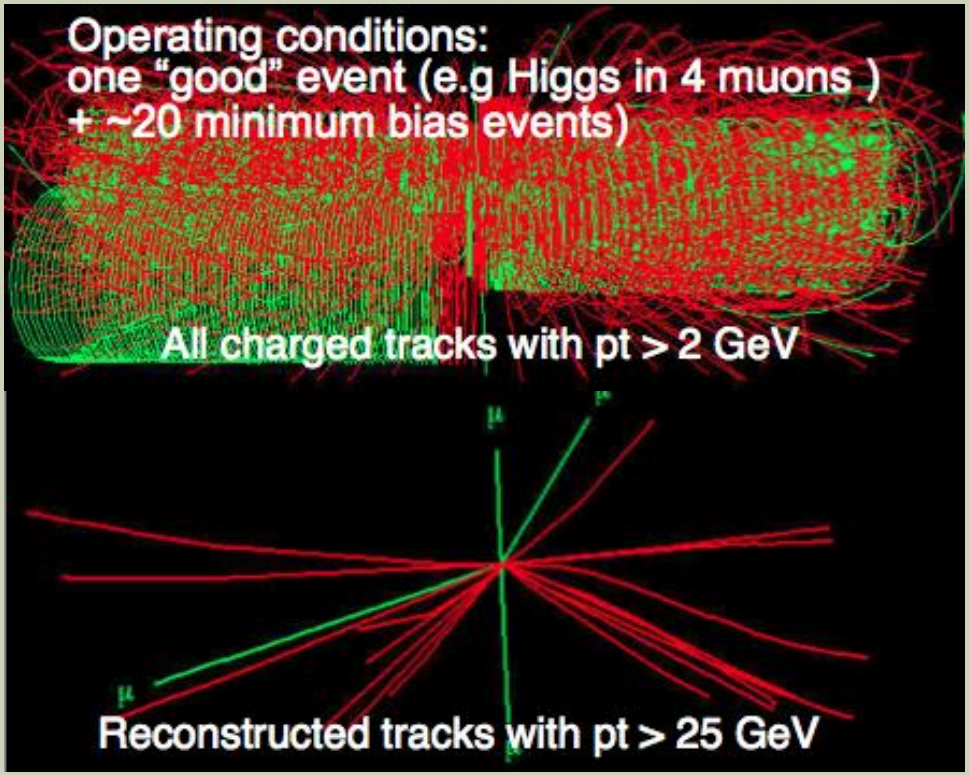
10^{35} $cm^{-2}s^{-1}$

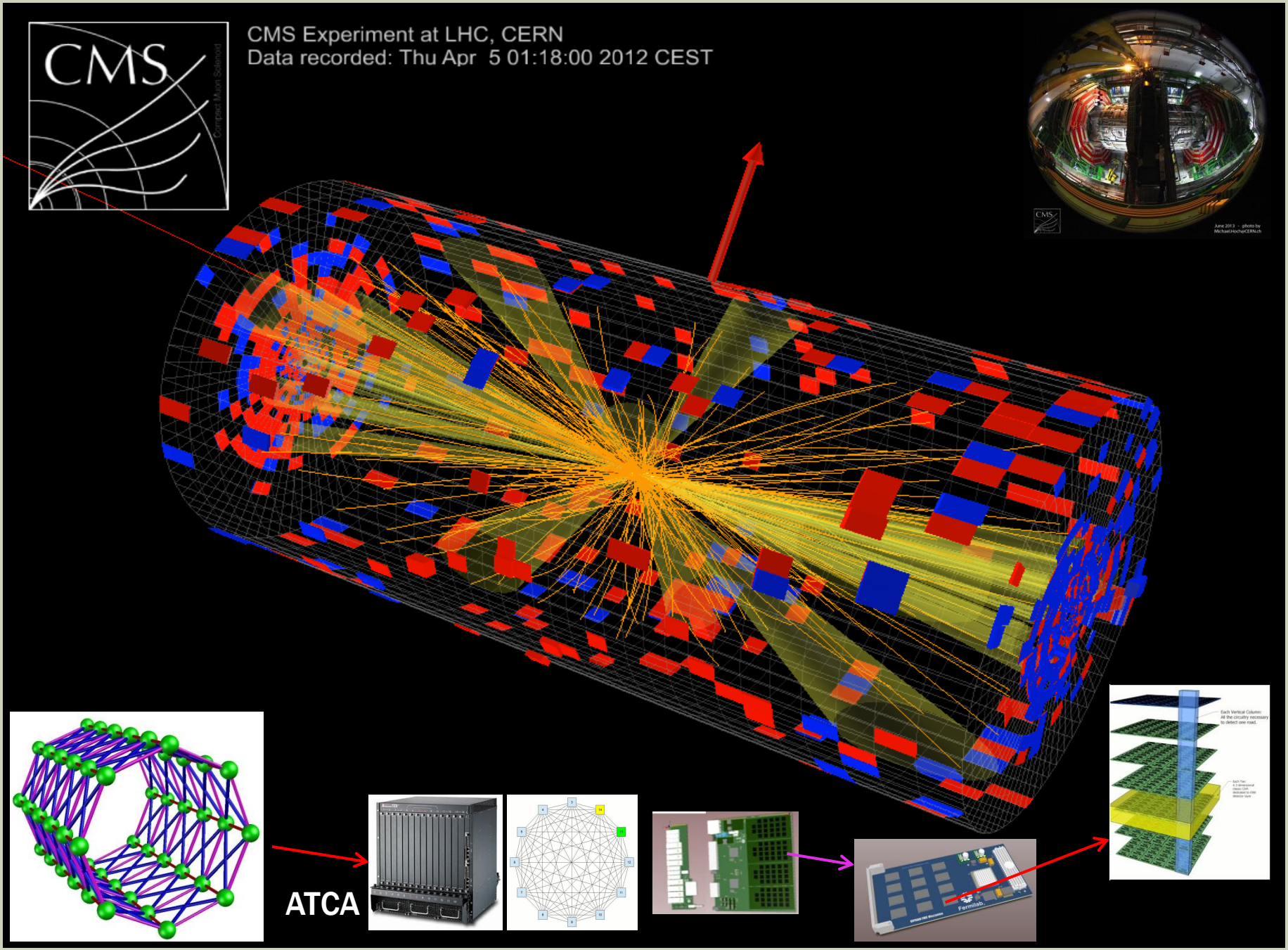


IMPACT OF L1 TRACKING TRIGGER

- CMS L1 Tracking Trigger:
  - Will need to reconstruct charged particle trajectories "on-the-fly" every 25 ns
  - An ocean of input data (bandwidth required to transfer up to ~ 50-100Tbps)
- Look-up Table
  - Compares known patterns to input data streams
  - Fast data communication and massive pattern recognition power

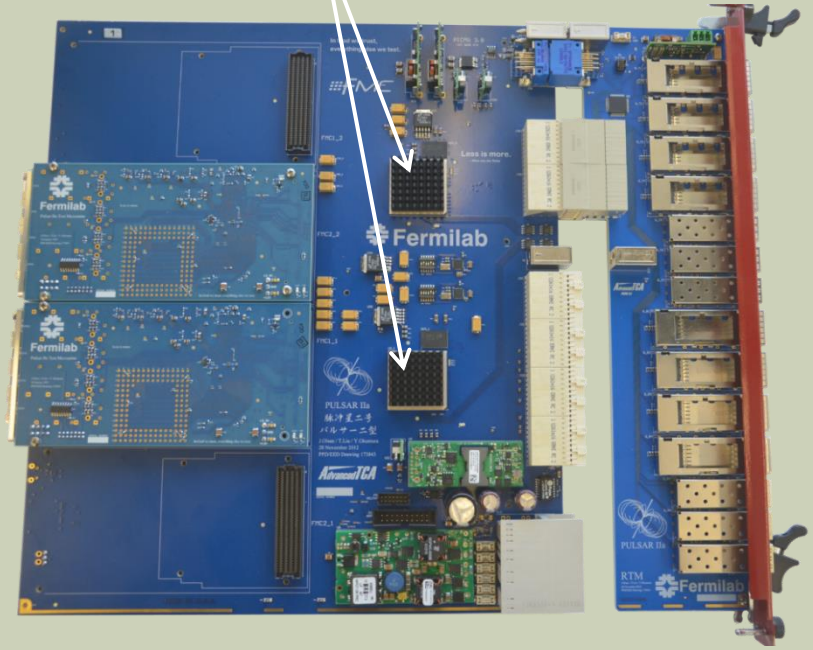
Pileup at HL-LHC: > ~ 140 (only 20 shown)

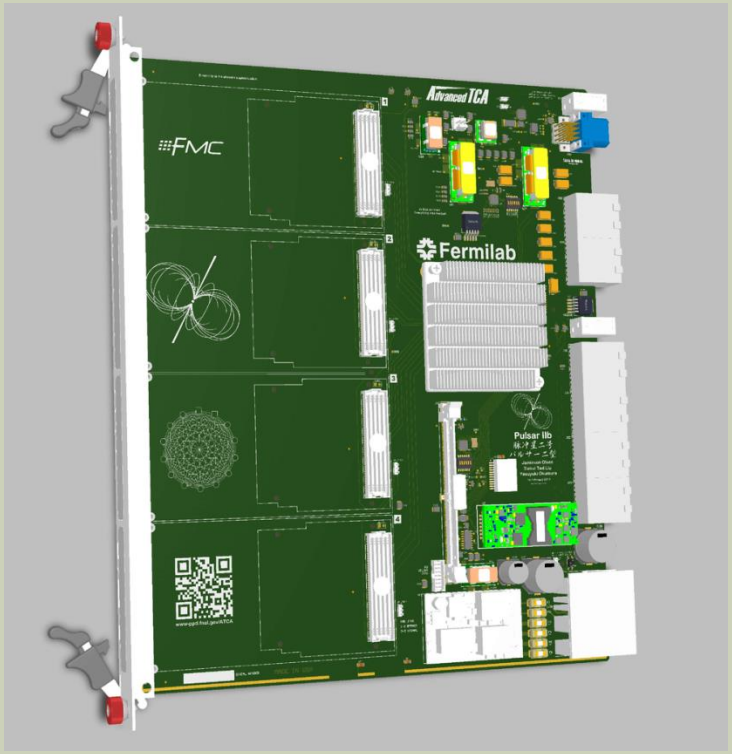



CMS
CMS Experiment at LHC, CERN
Data recorded: Thu Apr 5 01:18:00 2012 CEST
ATCA

PULSAR IIA AND PULSAR IIB

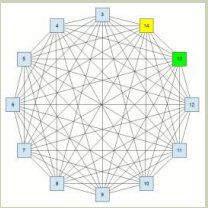
Pulsar IIa
(Kintex 7 FPGAs)



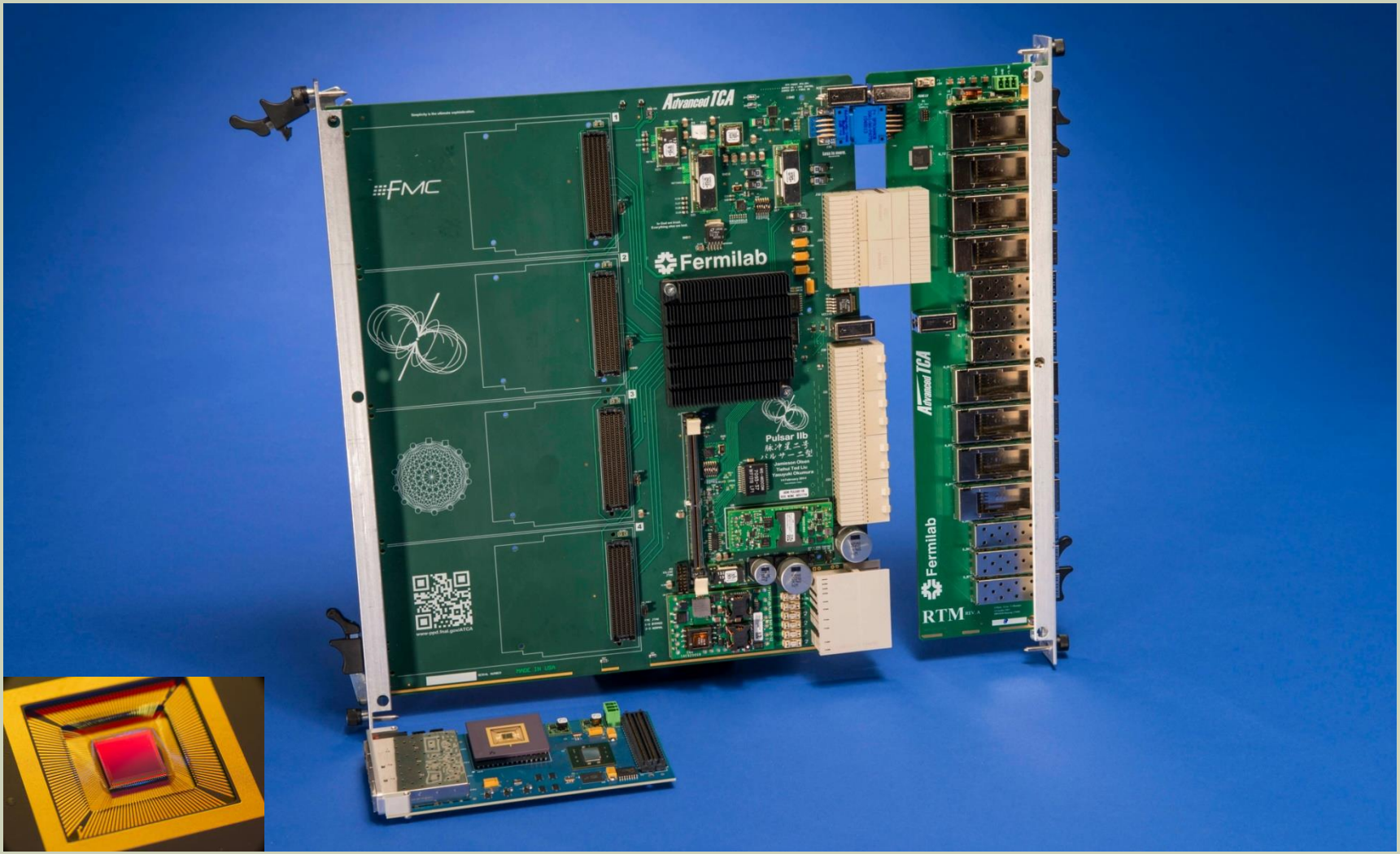


Pulsar IIb:

- Vertex 7 FPGA
- 80 GTH lines
- General purpose design

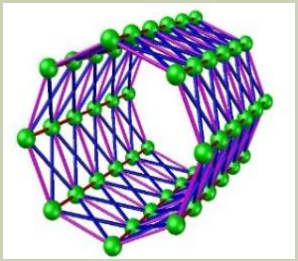


PULSAR IIB

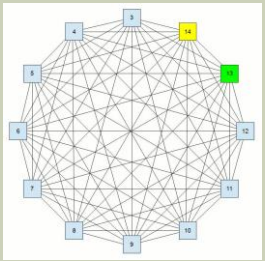

AdvancedTCA
FMC
Fermilab
Pulsar IIb
AdvancedTCA
Fermilab
RTM

HIGH SPEED LINKS IN PULSAR IIB

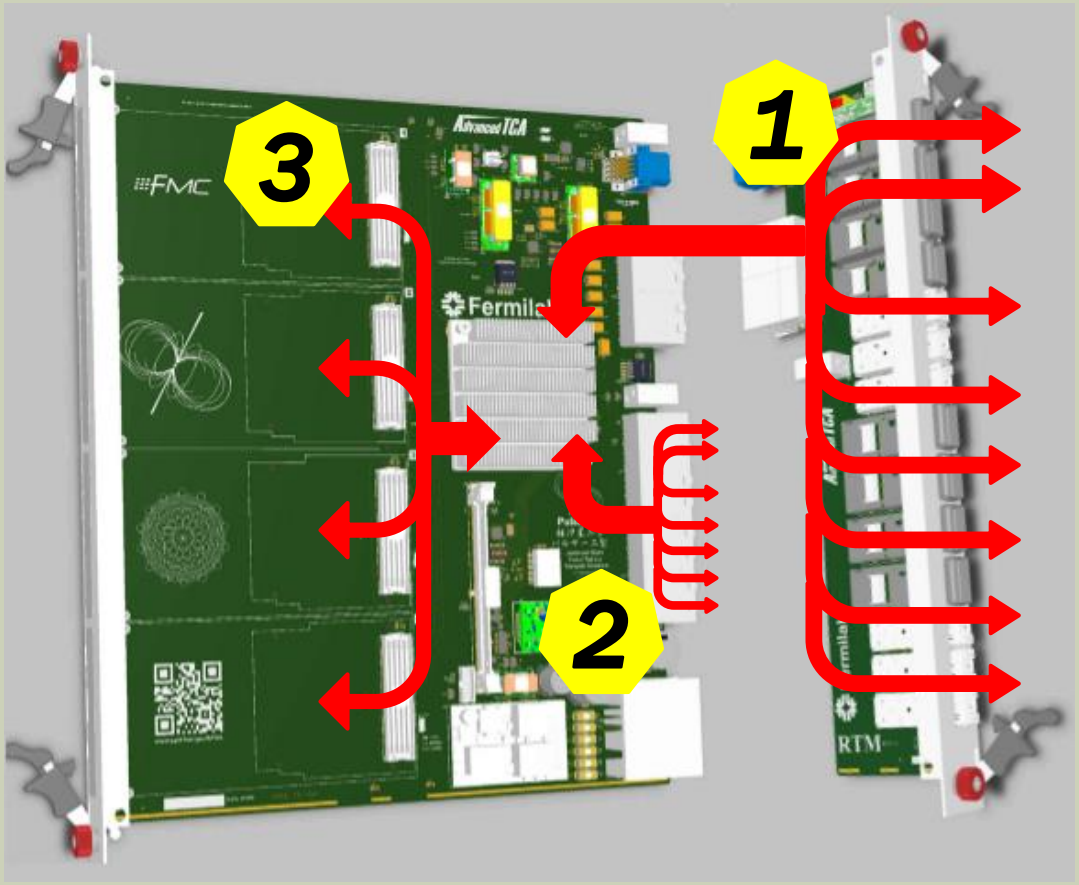
1) RTM + Optical fibers:



2) Full mesh backplane (fabric interface)

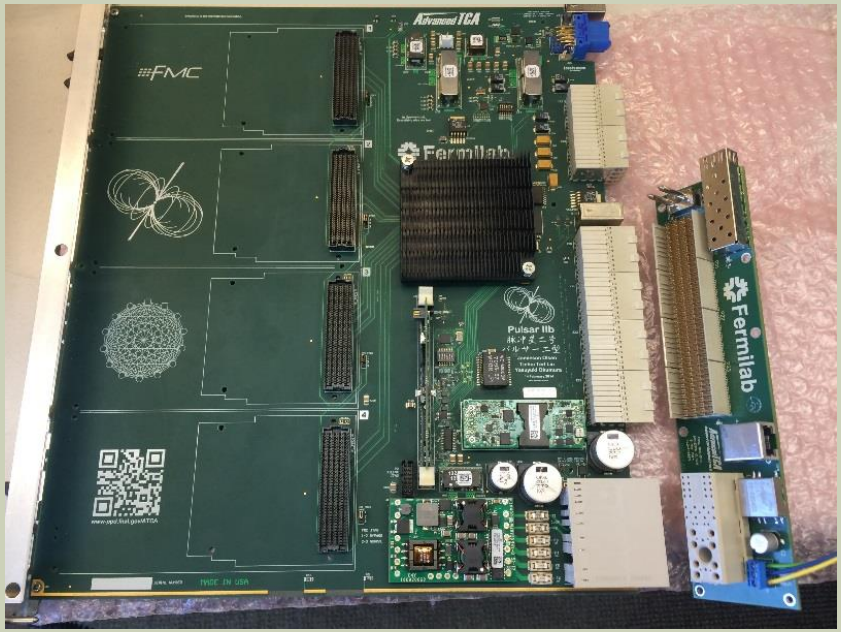


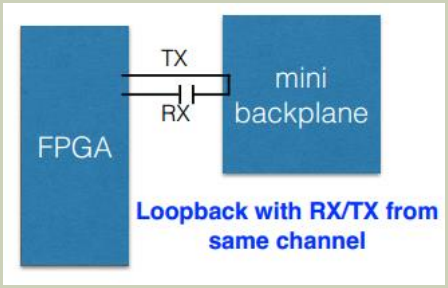
3) FMC interface

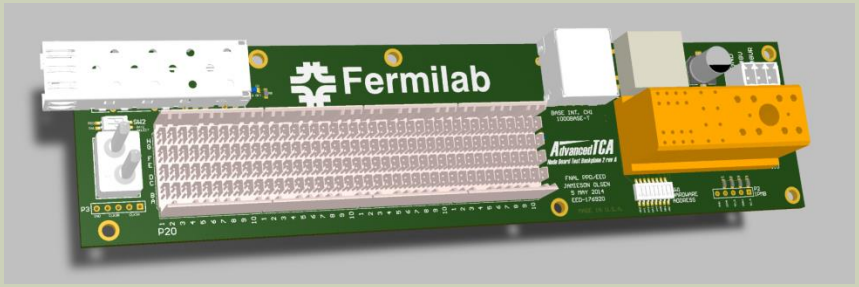


MINI BACKPLANE

- Used for Bench-level testing to test Pulsar II board by itself before testing with the full mesh backplane
- Loop back all fabric interface channels
- There are two versions of mini-backplane:
  - old and new

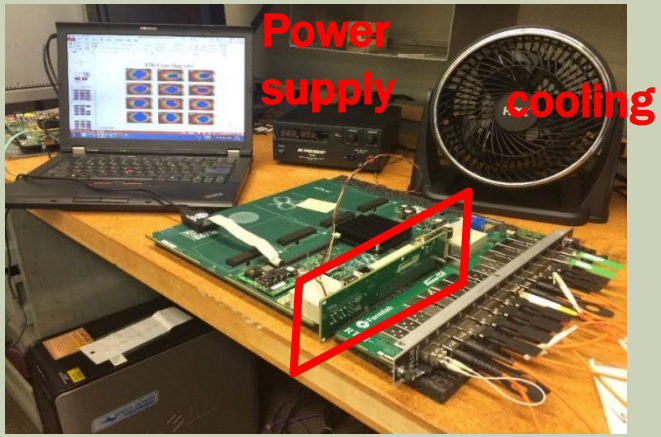






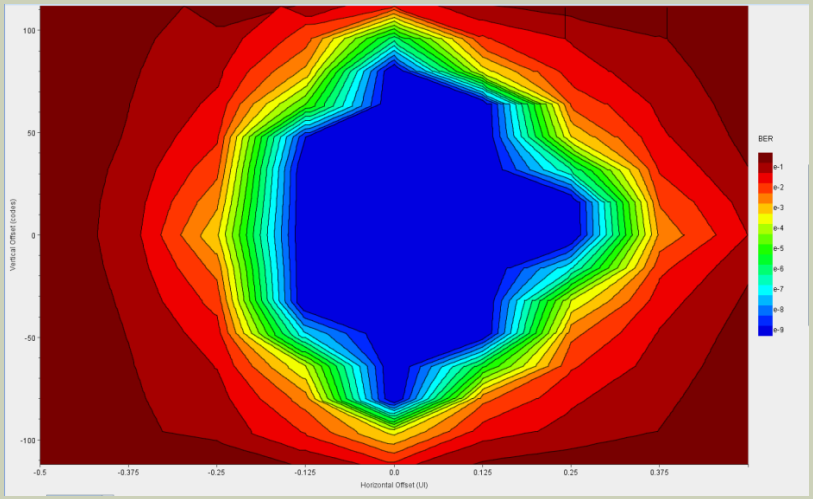
TESTING PROCESS

- Testing Process
  - Using a USB-JTAG Programming Cable, I was able to connect the board to the computer, ChipScope Pro Analyzer
  - Connection routes tested:
    - Local bus (Pulsar2A)
    - RTM
    - Mini-backplane (new and old)
    - Shelf (Board to Board by Full Mesh Backplane)
  - Tested at speeds of 6, 8, and 10 Gbps
  - Produced eye diagrams



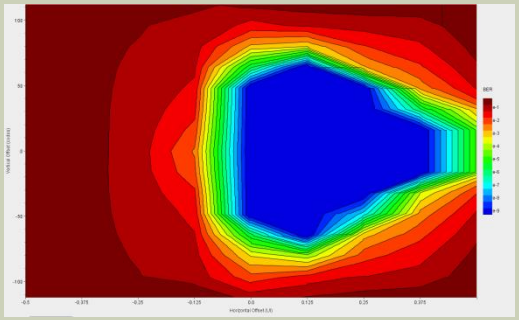
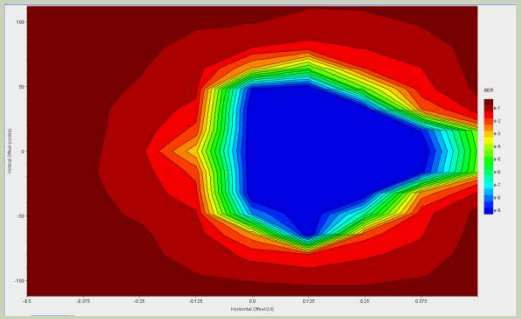
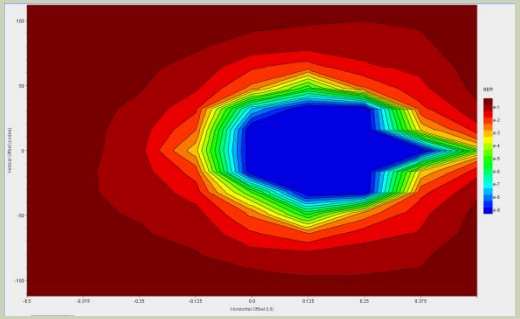
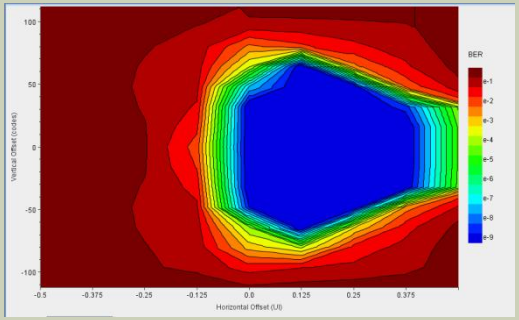
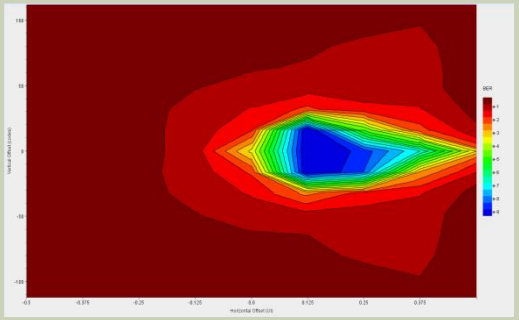
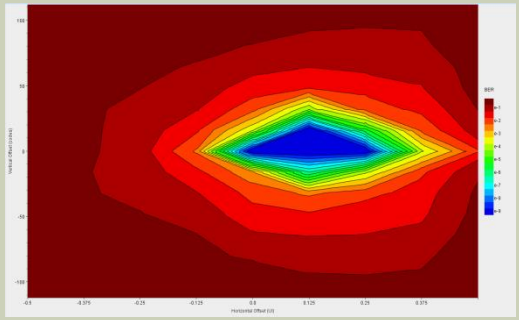
EYE DIAGRAMS

- IBERT tool provided by Xilinx to make eye diagrams for each high speed channel for Pulsar II
  - RX Margin Analysis (statistical eye)
    - The wider the blue eye, the better the link
    - X-axis: clock signal time offset
    - Y-axis: differential zero offset
    - Color: Log(BER)



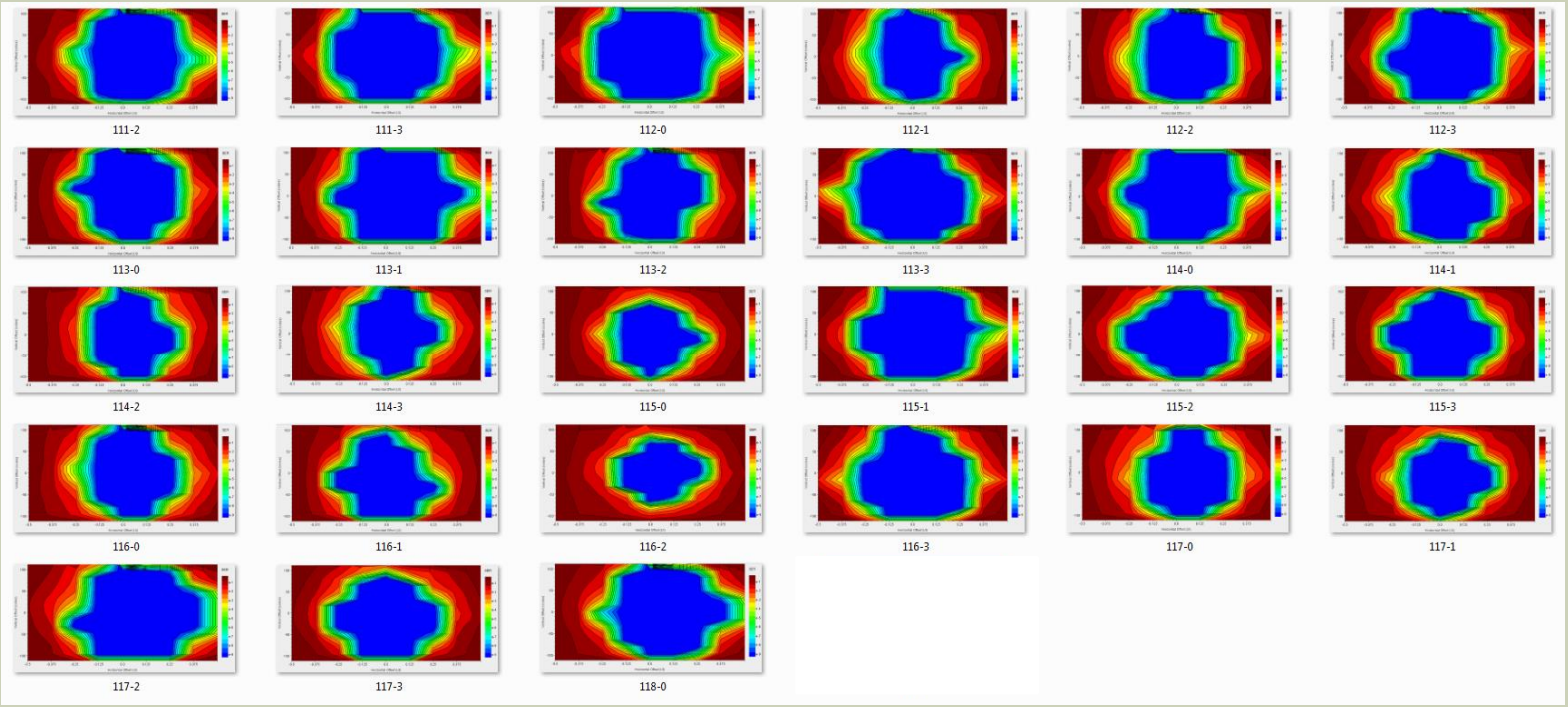
NEW V. OLD MINI-BACKPLANE

- At all speeds: testing with Pulsar IIa
  - New is better than the old, especially at higher speeds (X0Y6_Top)
  - This means that the new mini-backplane can be used for testing Pulsar IIb

	6.25 Gbps	8.00 Gbps	10.00 Gbps
New			
Old			

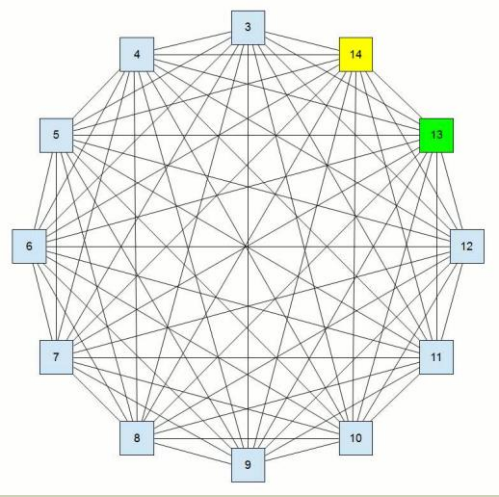
MINI-BACKPLANE LOOPBACK

- Fabric interface channels work well with mini-backplane loopback, Pulsar IIb at 10 Gbps
- Pulsar IIb can be used to measure and scan the performance of an ATCA full-mesh backplane

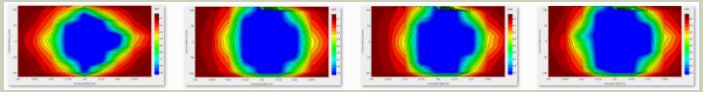


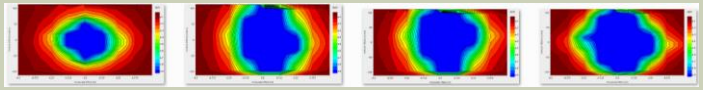
ATCA FULL MESH BACKPLANE TESTING

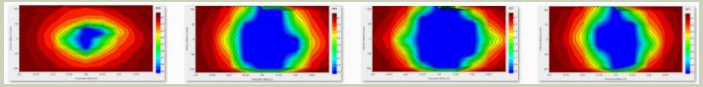
- Testing procedure:
  - 2 slots at a time, check the direct links
  - Scan all the full mesh network
- Tested two shelves at 10Gbps
  - Pulsar IIb uses 2 lanes per channel

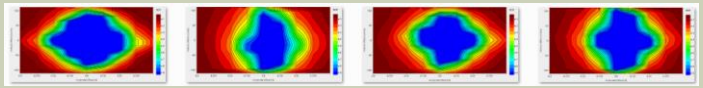


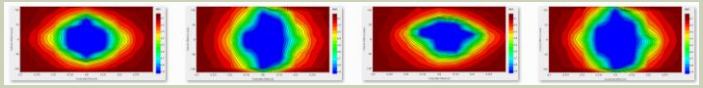
SHELF A AT 10GBPS

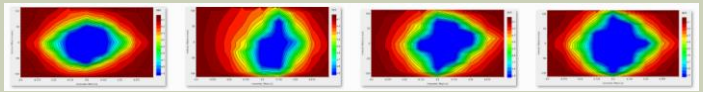
#1↔#2 

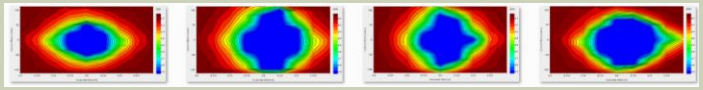
#1↔#3 

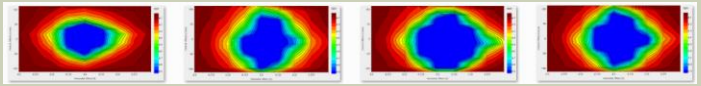
#1↔#4 

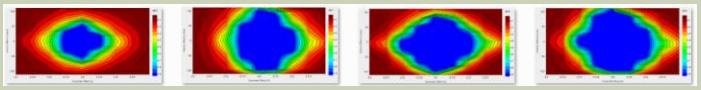
#1↔#5 

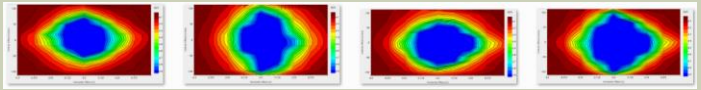
#1↔#6 

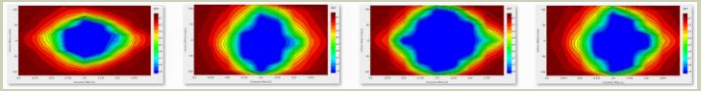
#1↔#7 

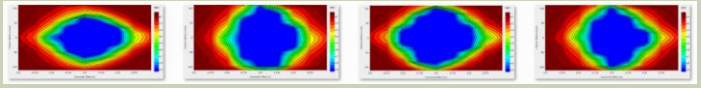
#1↔#8 

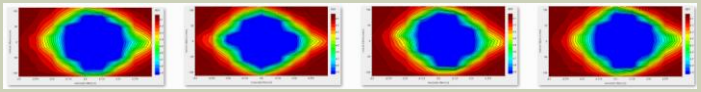
#1↔#9 

#1↔#10 

#1↔#11 

#1↔#12 

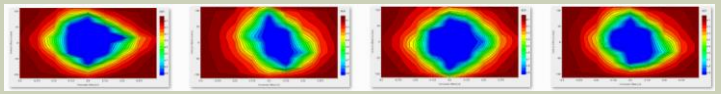
#1↔#13 

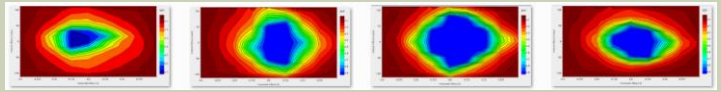
#1↔#14 

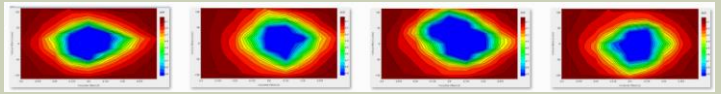
#1↔#14

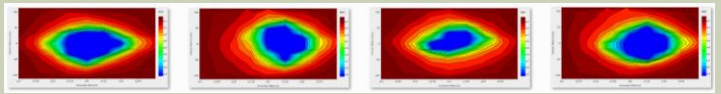
Slot # from left to right: #1, #2, #3 … #14

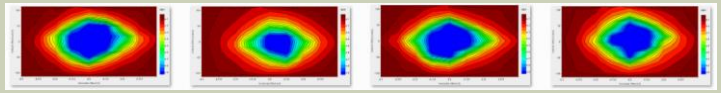
SHELF B AT 10GBPS

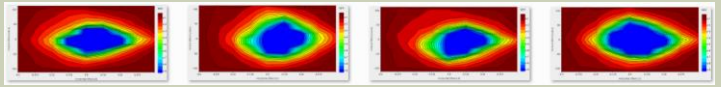
#1↔#2 

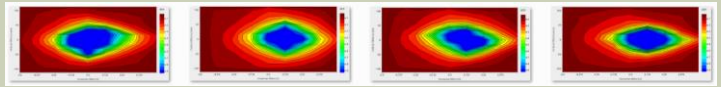
#1↔#3 

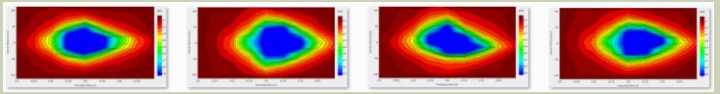
#1↔#4 

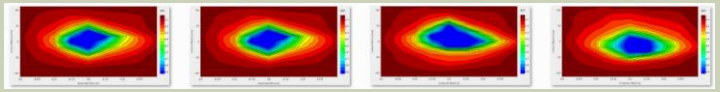
#1↔#5 

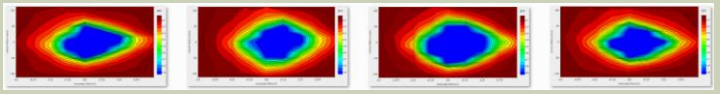
#1↔#6 

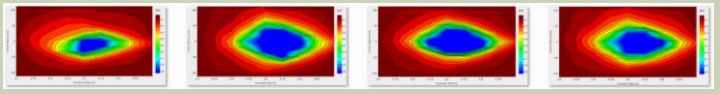
#1↔#7 

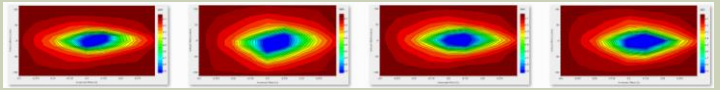
#1↔#8 

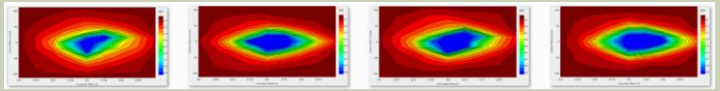
#1↔#9 

#1↔#10 

#1↔#11 

#1↔#12 

#1↔#13 

#1↔#14 

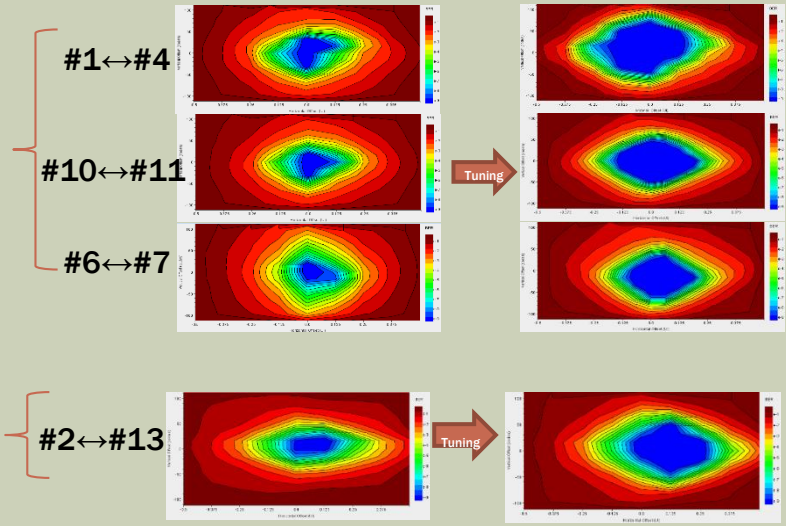
Slot # from left to right: #1, #2, #3 … #14

TUNING

- Performance affected by:
  - Transmission media
  - Receiver (RX) and Transmitter (TX) parameters
- By tuning TX/RX parameters, channel performance can be improved
  - TX differential swing voltage,
  - TX pre/post-cursor emphasis
  - Termination voltage

ATCA SHELVES TEST SUMMARY

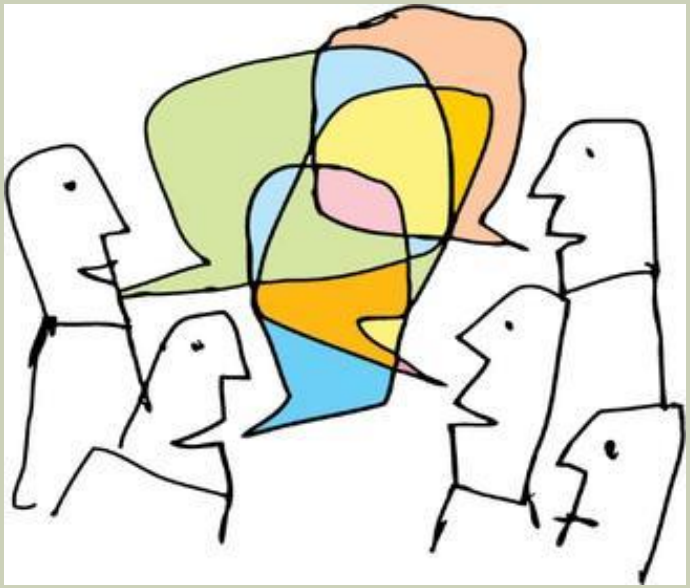
- Shelf A:
  - 3 small eyes are found
  - independently tuned
- Shelf B:
  - Many poor channels are found
  - After tuning, the eye is still small or shifted to one side

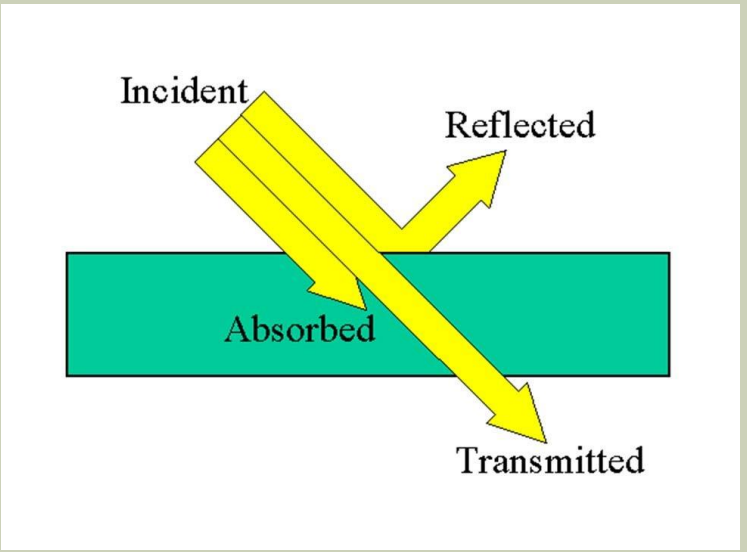


- Shelf A has a better backplane than Shelf B
- One more shelf is on the way to FNAL for evaluation

SIGNAL TRANSMISSION EFFECTS

- Transmission performance affected by loss, reflection, and crosstalk





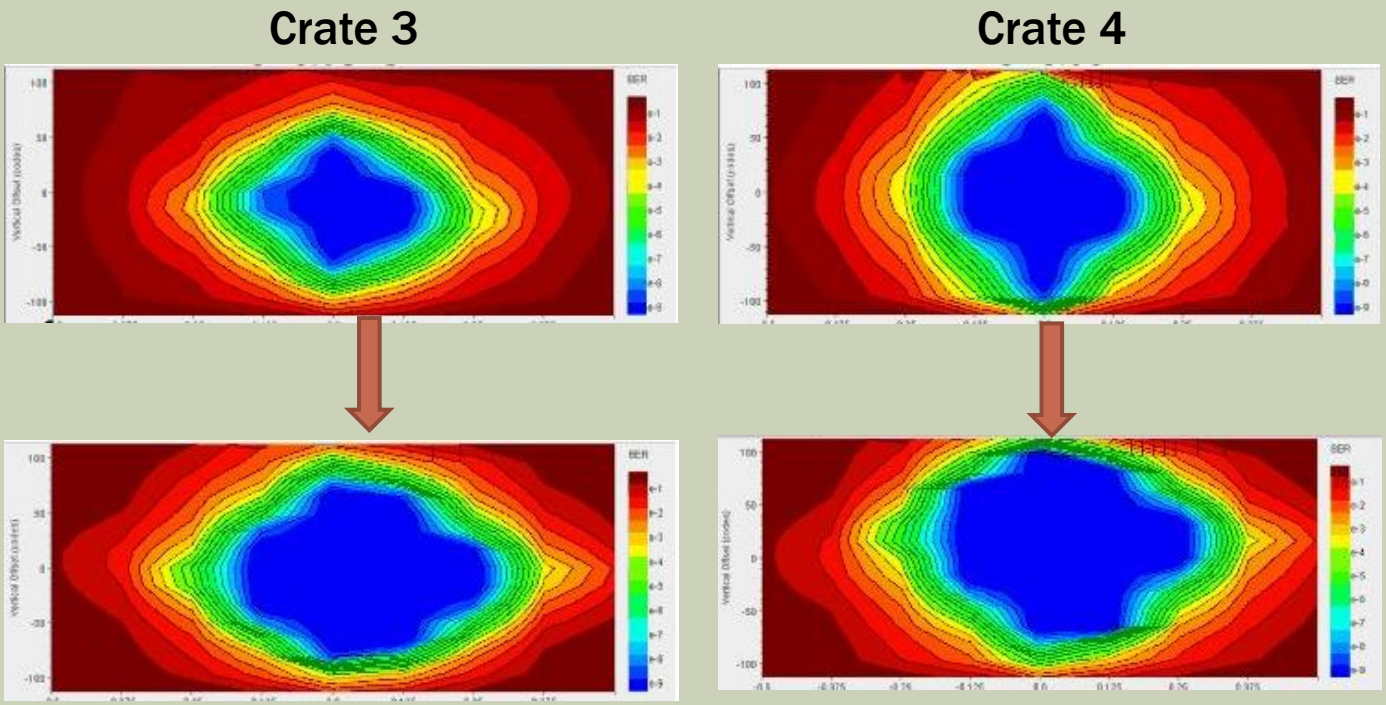
XILINX ADVANCED REFLECTION CANCELLATION

- XARC only available for GTH (Pulsar2B)
- Transmission effects on backplane
  - Loss can occur in links and connections
  - Reflection can occur in the connector
  - Crosstalk can occur in links close together

- XARC will reduce effects from reflection

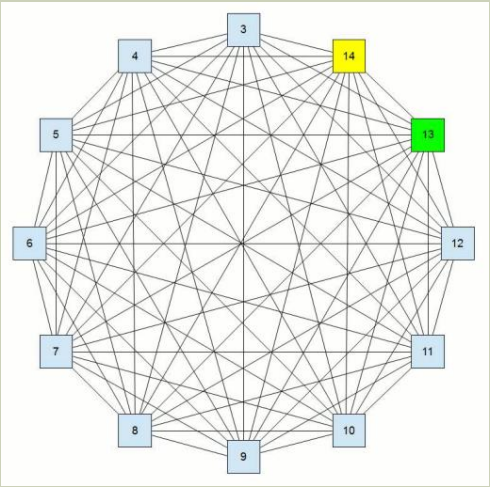
CRATE LEVEL TEST

XARC results at 10 Gbps, channel 116_2



PULSAR IIB FUTURE

The next milestone is to test the full mesh backplane with many Pulsar IIb boards.



EXPERIENCE AT FERMILAB

- What I learned:
  - Basic ideas of high speed communication system, how board connections work
  - CMS, LHC
- True working experience
- Science Research Class in MTHS

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